

# 915P-M3

Rev: 1.0

Page Title of Schematic :

Schematics Version History Table :

Circuit Ver.	PCB Ver.	Total Page	Modified Page(s)	Date
A	A	36		11/02/' 04
1.0	1.0	36		12/15/' 04
1.0	1.0			03/25/' 04

Title	Page	Title	Page
Cover Sheet	1		
System Block Diagram	2		
P4 LGA775P Part A	3		
P4 LGA775P Part B	4		
P4 LGA775P Part C	5		
P4 LGA775P Part D	6		
P4 LGA775P Part E	7		
Clock Generator(CK410)	8		
I-GSD(MCH)Part A & E & F	9		
I-GSD(MCH)Part D	10		
I-GSD(MCH)Part B & C	11		
I-GSD(MCH)Part G	12		
DDIMM 1&2 ( DDR SDRAMs )	13		
DDIMM 3&4 ( DDR SDRAMs )	14		
DDR & V_FSB_VTT Power	15		
PCI EXPRESS 16-PORT	16		
ICH6 Part A & D (SATA-CONNECTOR)	17		
ICH6 Part B & C (RTC)	18		
ICH6 Part E & F (POWER & GND)	19		
IDE1 Connector	20		
USB/FWH	21		
LPC_FDD/KB/M	22		
I/O Ports	23		
H/W Monitor	24		
AC97 Codec	25		
Audio Interface	26		
ATX Power & Front Panel	27		
LAN	28		
Vcore DC-DC	29		
MIS DC-DC(DUAL & VDDQ)	30		
PCI Slot 1&2	31		
PCI Slot 3	32		
Back I/O	33		
VT6307 (1394)	34		
TPM (TRUSTED PF-MODELE)	35		
Schematic Change History	36		

DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1
PCI3	19	F/E/H/G	PREQ-2	PGNT-2
1394	20	D	PREQ-3	PGNT-3
LAN	21	E	PREQ-4	PGNT-4

PCB : 244 x 244 mm ; 4 layers

**INTEL  
P4 Processor  
PSC, Tejas -  
LGA 775 pin**

BW : 4.1GB/s @ FSB : 533MHz & Freq : 133MHz  
BW : 6.4GB/s @ FSB : 800MHz & Freq : 200MHz

SIZE : Min 128MB (ONE 256Mb X 16 Single-Sided DEVICES)  
SIZE : Max 4GB (Four 512Mb X 8 Double-Sided DEVICES)  
BW : 8.5GB/s @ DDR2 :400/533MHz  
BW : 6.4GB/s @ DDR : 333/400MHz

**INTEL  
i915GV  
1210pin FC-BGA**

**DDIMM1: DDR Socket 184P**  
**DDIMM2 : DDR Socket 184P**  
**DDIMM3: DDR Socket 184P**  
**DDIMM4 : DDR Socket 184P**

**VGA (G only)**

Analong Display  
RAMDAC: 400MHz  
Resolutions Up To 2048x1536@75Hz

BW : 2GB/s (Support Lsoch)

**USB1  
2 ports** **USB2  
2 ports** **USB3  
2 ports** **USB4  
2 ports** **USBLAN  
8 ports**

USB V2.0

**PCIEx1**

**INTEL  
ICH6  
609pin EPGA**

BW : 133MB/s @Freq : 33MHz

**PCI1 Slot 120pin @ AD17**  
**PCI2 Slot 120pin @ AD18**  
**PCI3 Slot 120pin @ AD19**

**IDE1 40pin**  
Up to Ultra ATA/100  
Two IDE Channel

**Line in**  
**Line out**  
**Mic in**  
**Center/Bass out**  
**Surround**  
**Side-Surround**

**Audio Codec  
ALC880**

AC' 97 & Lan I/F

LPC bus

**SATA1 7Pin**  
**SATA2 7pin**  
**SATA3 7Pin**  
**SATA4 7pin**

BW : 150MB/s

**intel  
FWH  
32pin PLCC**

**TPM 1.1**

**Super I/O  
W83627THF  
128pin PQFP**

**VIA 1394  
(OPTION)**

**10/100  
Lan**

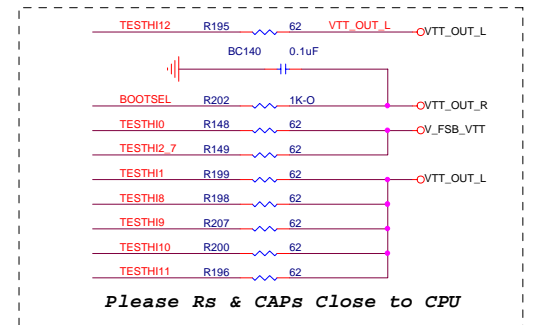
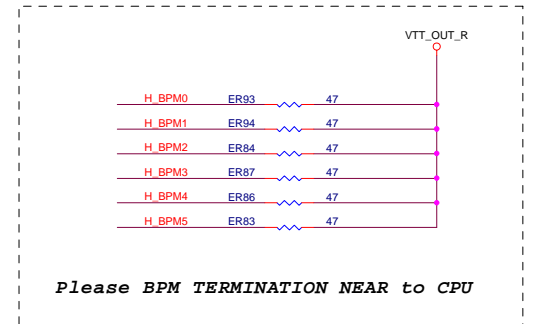
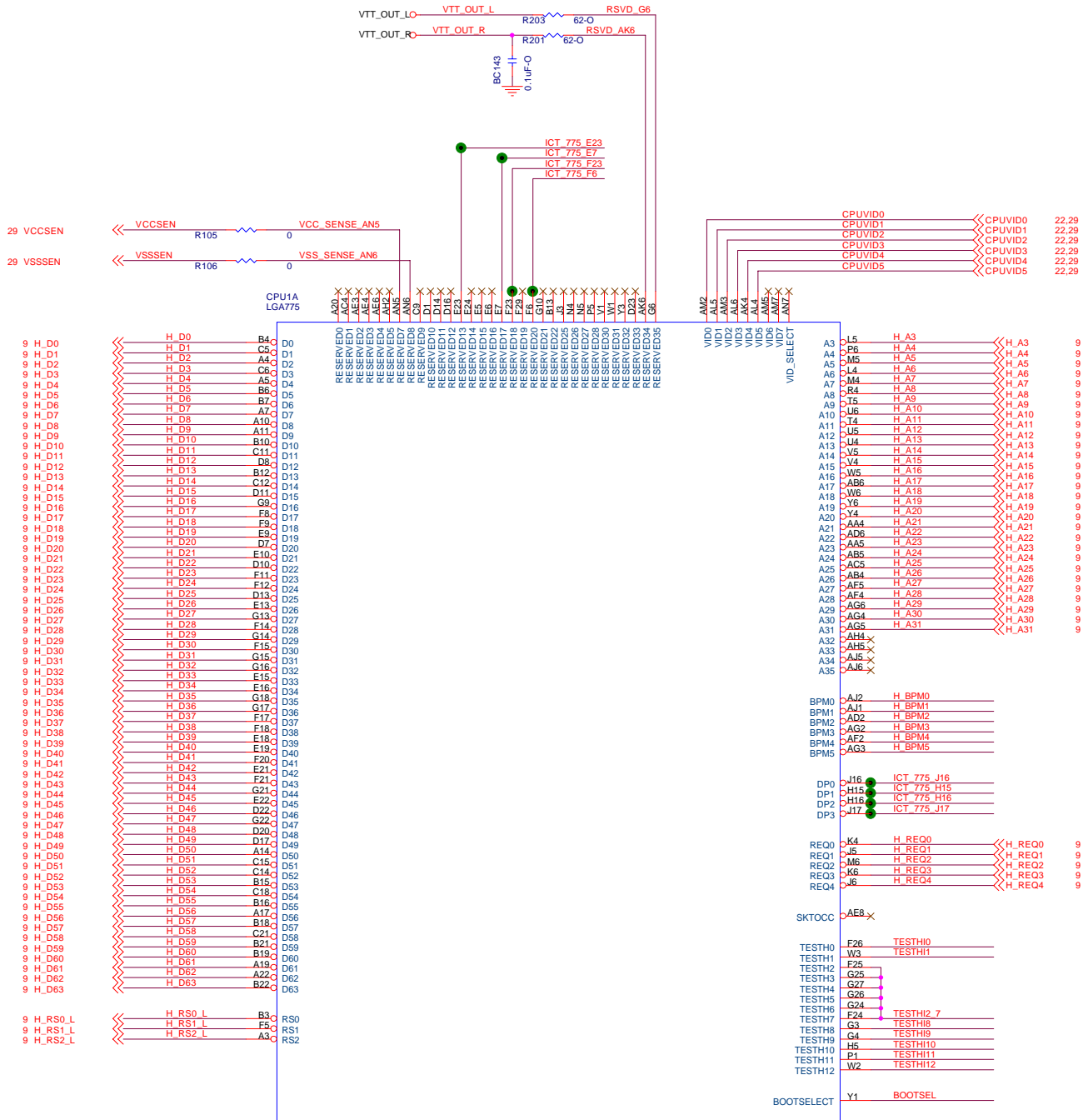
**USBLAN  
RJ45**

**CONN/  
HEADER**

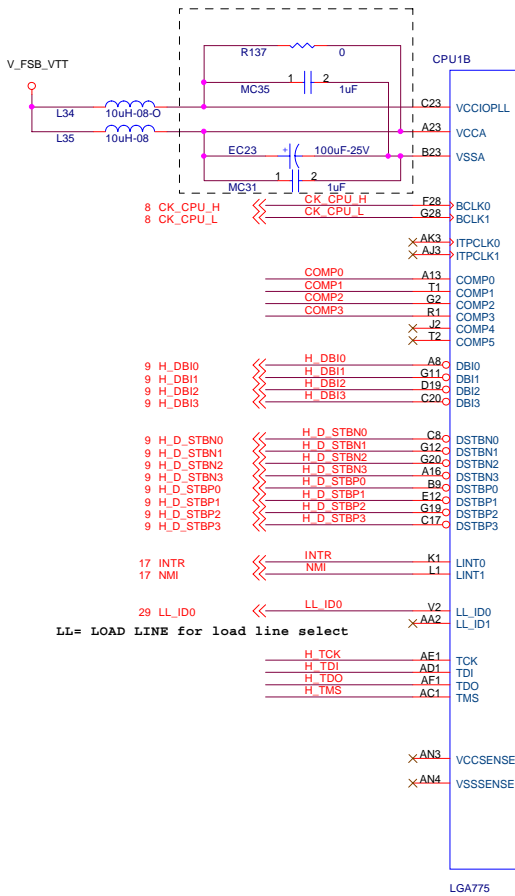
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**System Block Diagram**

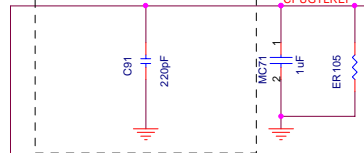
Size B Document Number **915G-M3** Rev 1.0  
Date: Friday, March 25, 2005 Sheet 2 of 36



Place componets as close as possible to Processor socket  
trace width to cap must be no smaller than 12 Mils

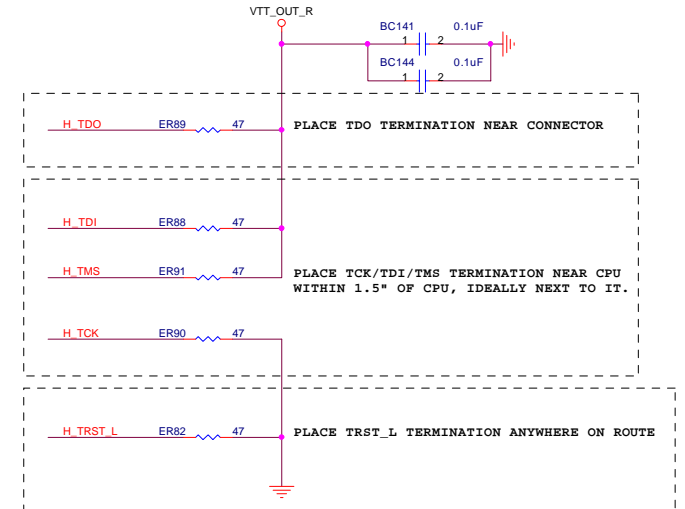
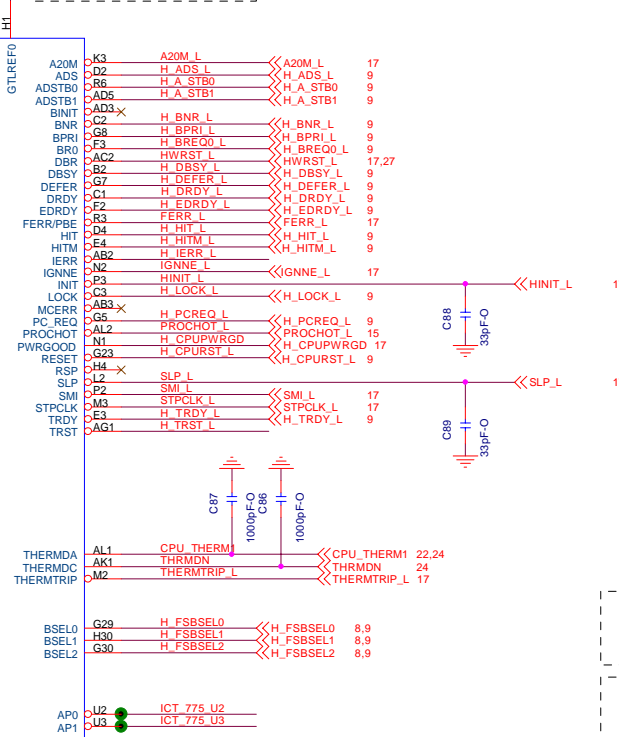
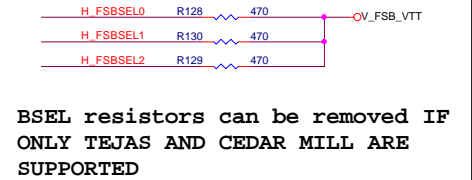
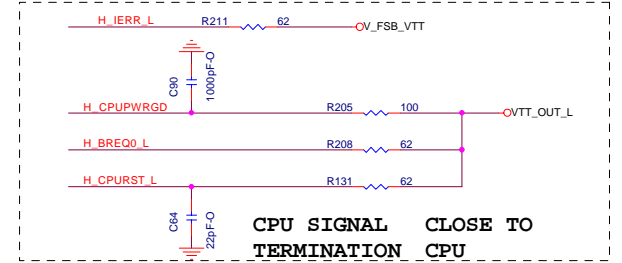


Close CPU H1 pin

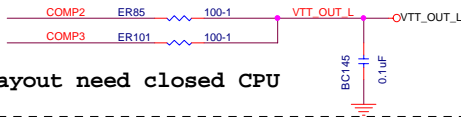


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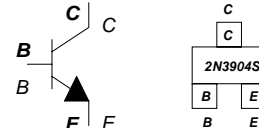
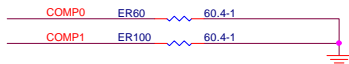
GTLREF GENERATION CIRCUITS



Layout need closed CPU



Place outside Socket Cavity

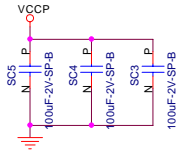
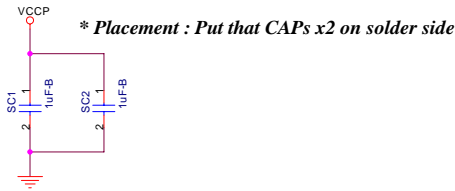
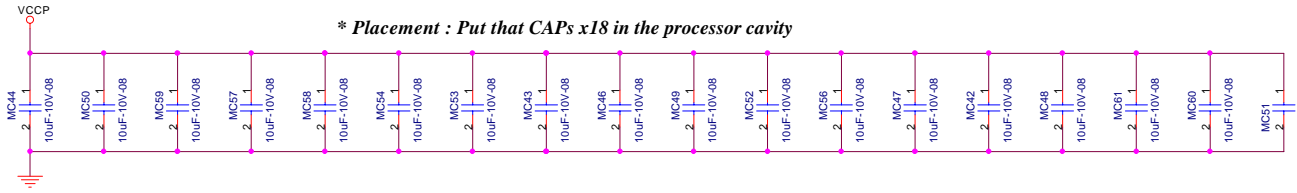


itegroup Computer Systems		
Title <b>P4 LGA775P Part B</b>		
Size	Document Number	Rev
Custom	<b>915G-M3</b>	<b>1.0</b>
Date:	Friday, March 25, 2005	Sheet 4 of 36

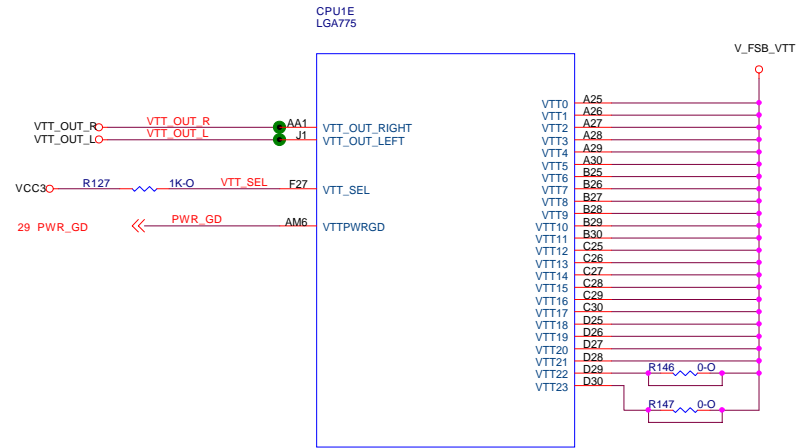


CPU1C  
LGA775

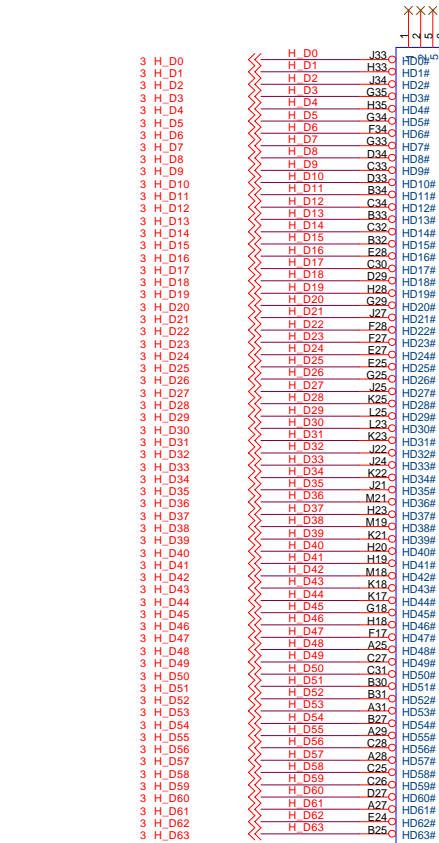




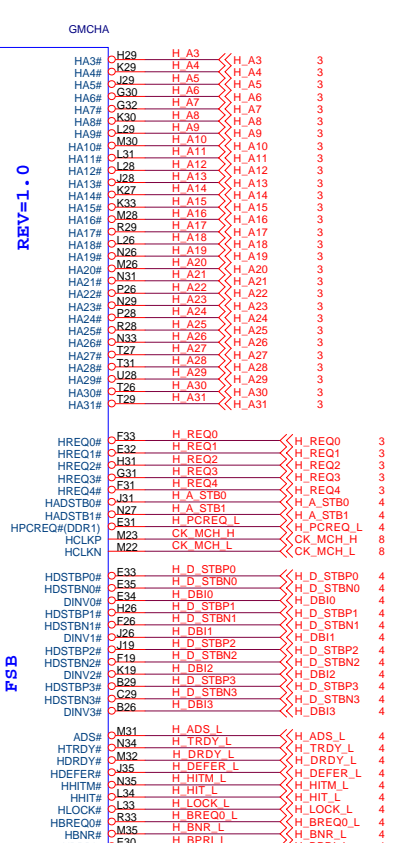
VTT\_SEL=0 for the Tejas processor



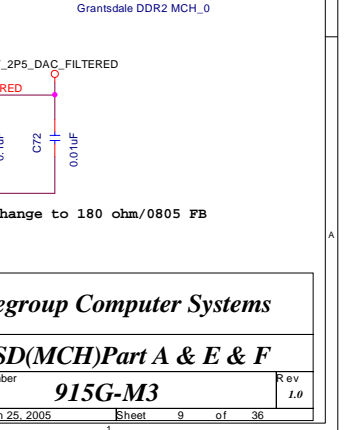
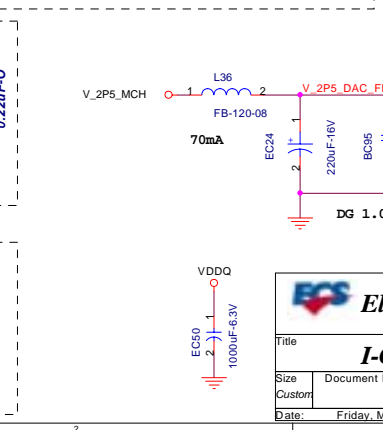
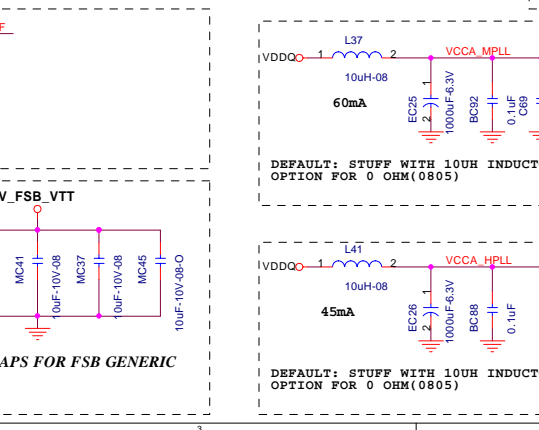
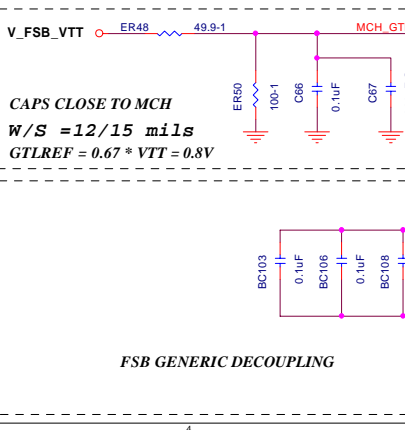
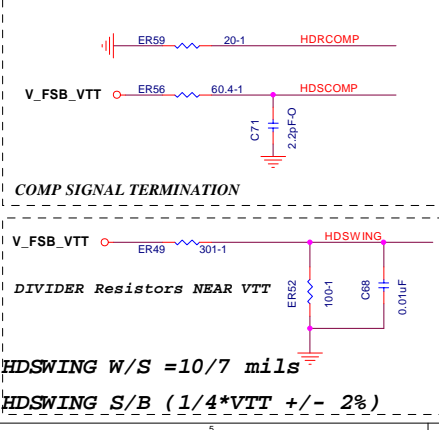
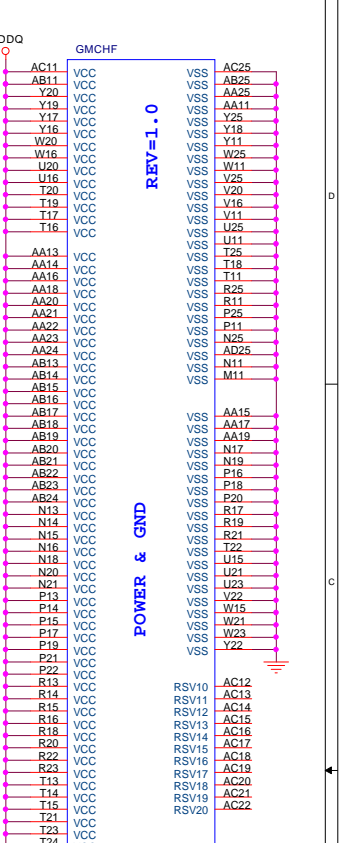
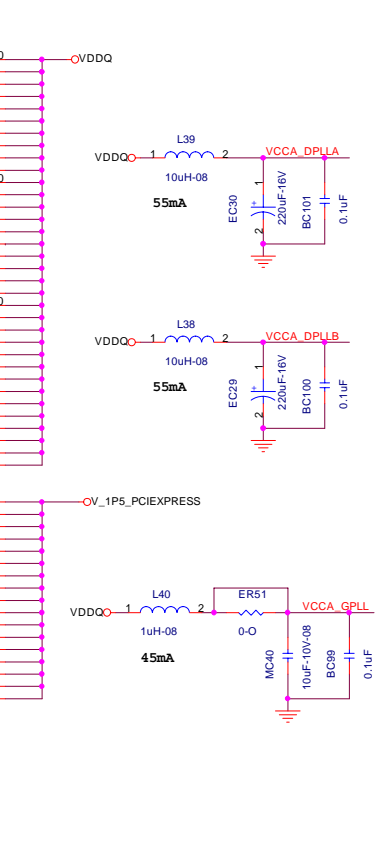
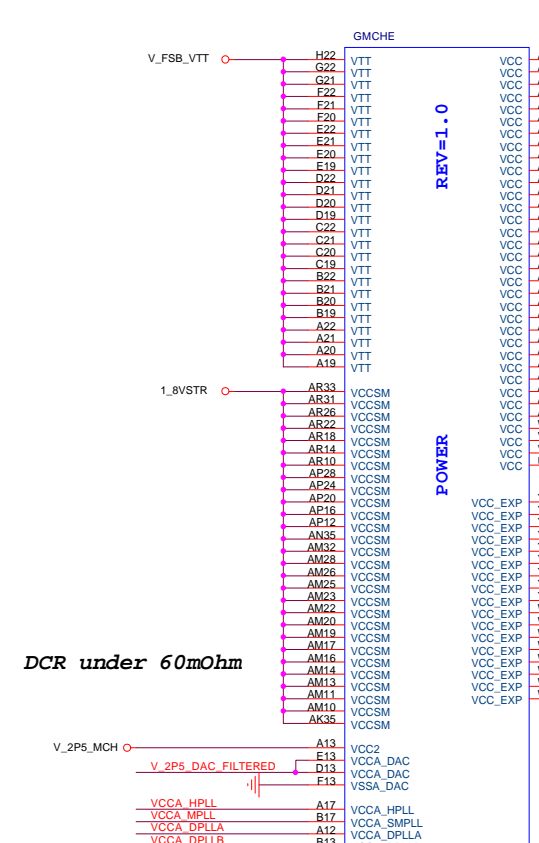




BSEL TABLE			
2 1 0 PSB FREQUENCY			
0 0 1 133 MHZ (533)			
0 1 0 200 MHZ (800)			

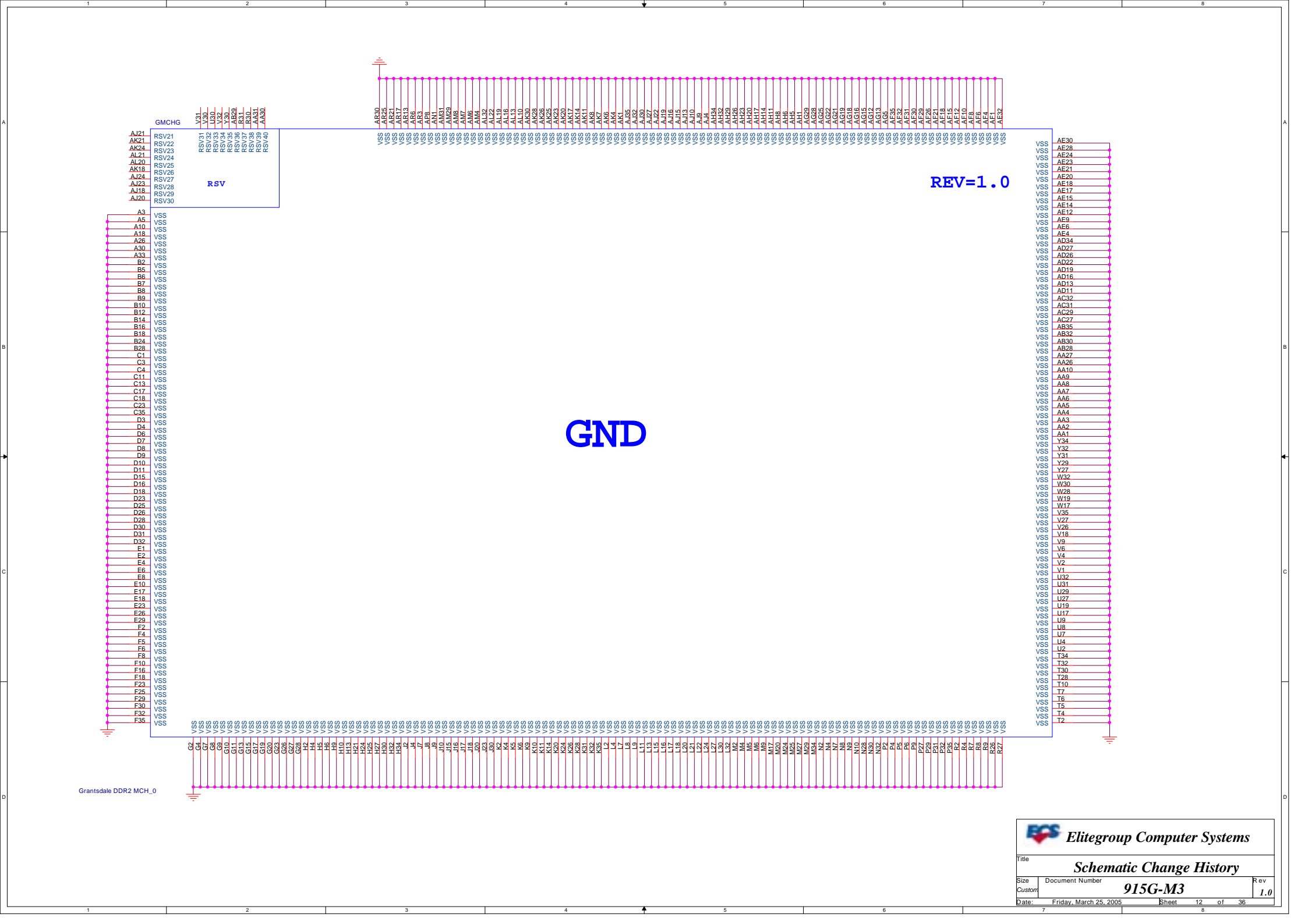


BSEL TABLE			
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0 0 1 133 MHZ (533)			
0 1 0 200 MHZ (800)			

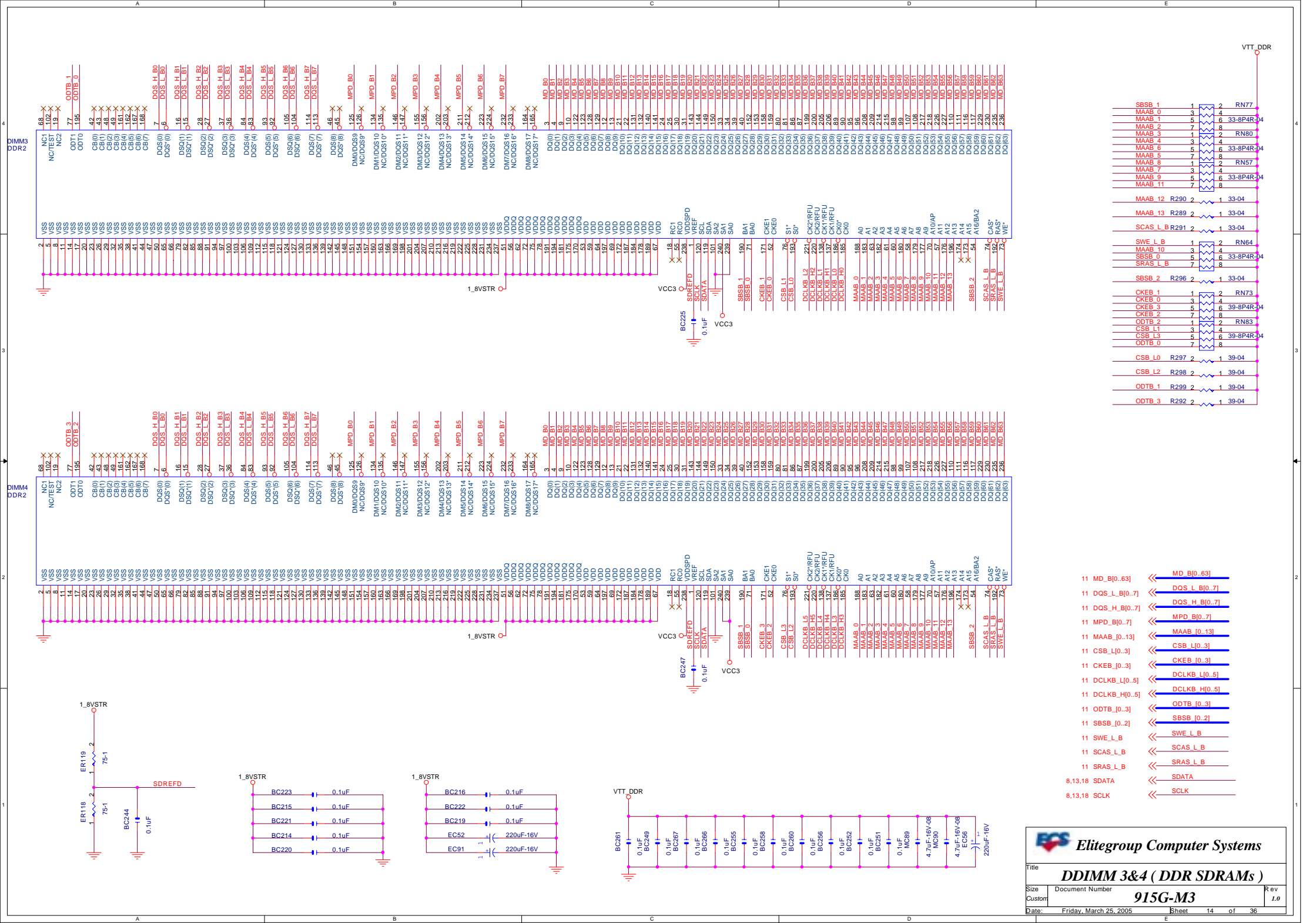


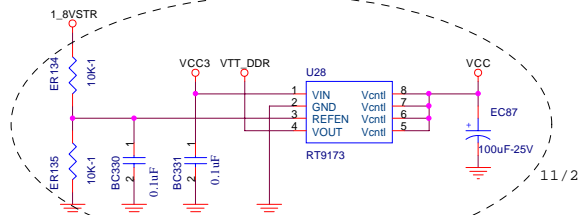




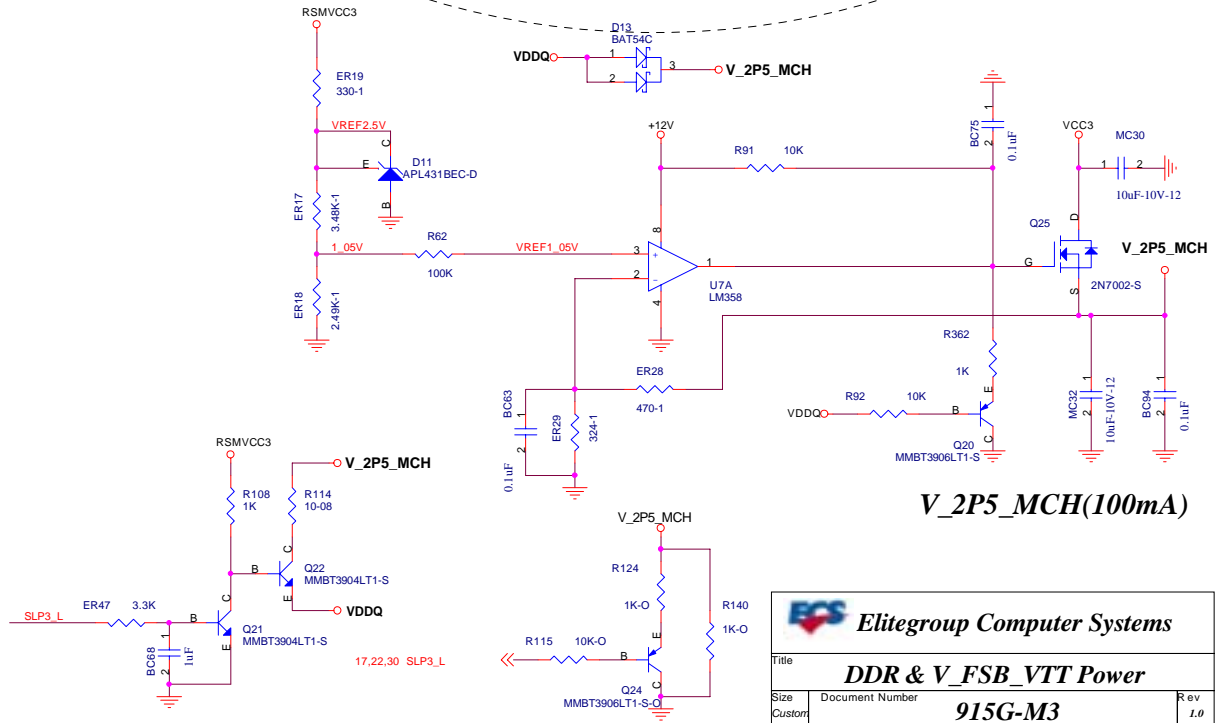
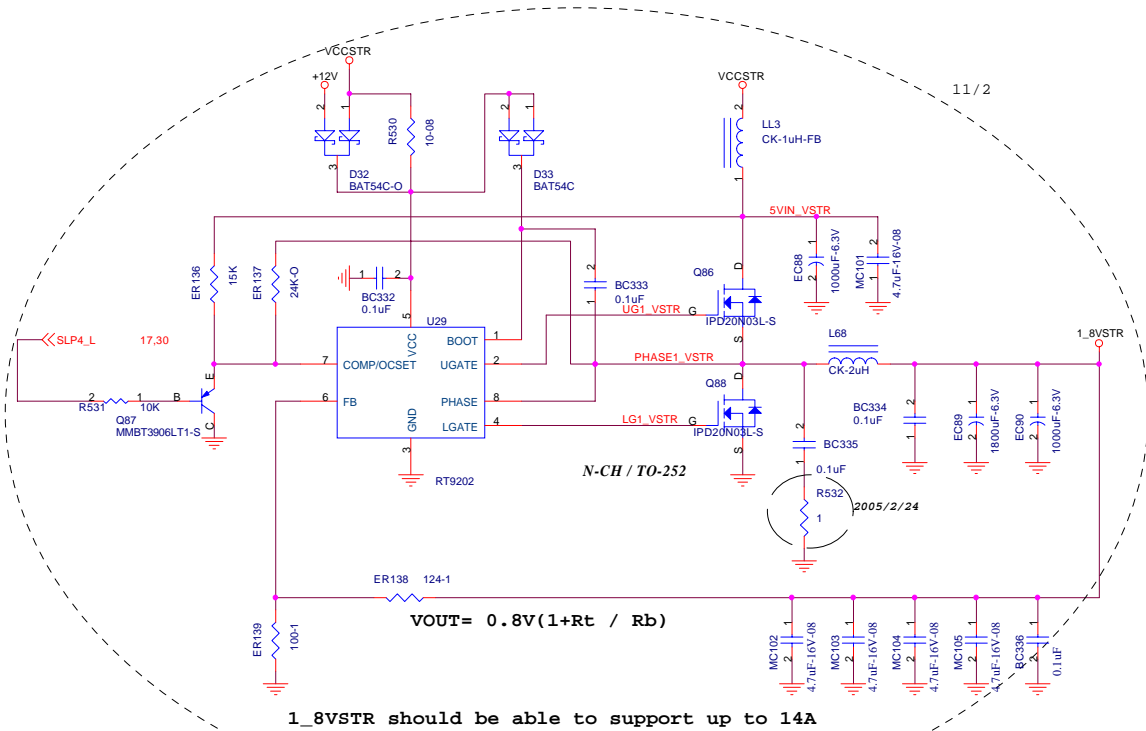
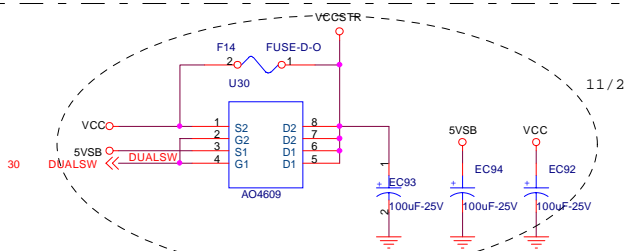
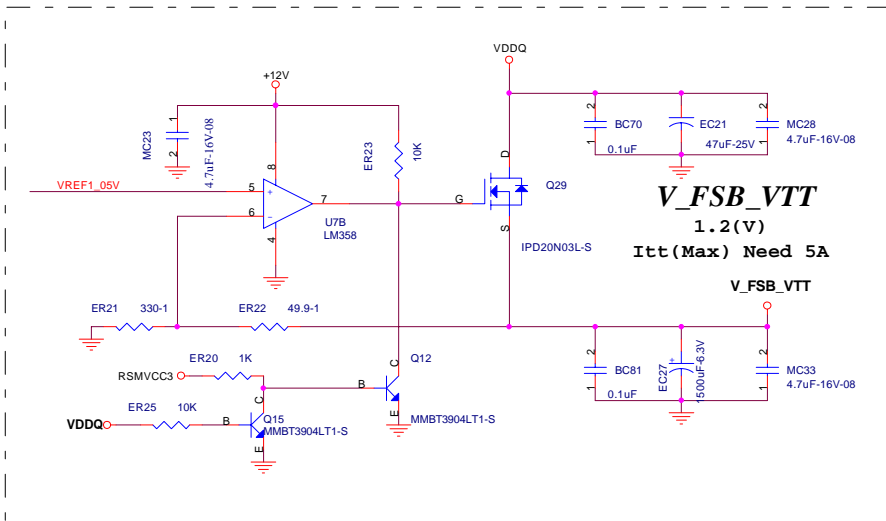
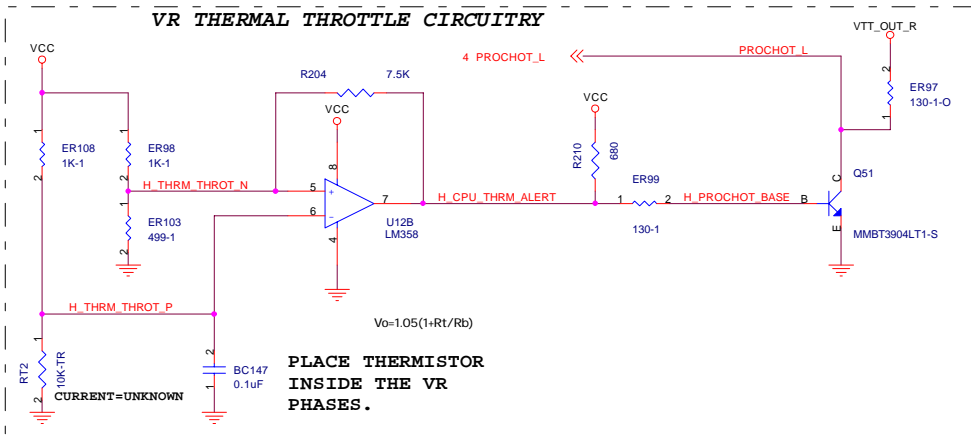








### VR THERMAL THROTTLE CIRCUITRY

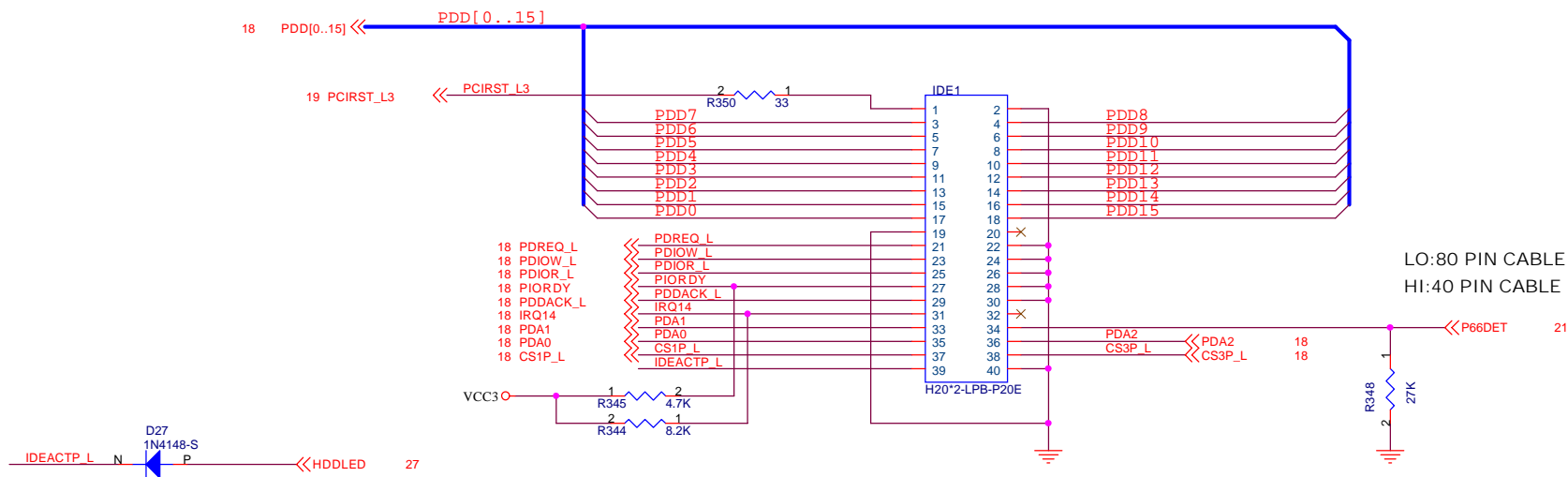








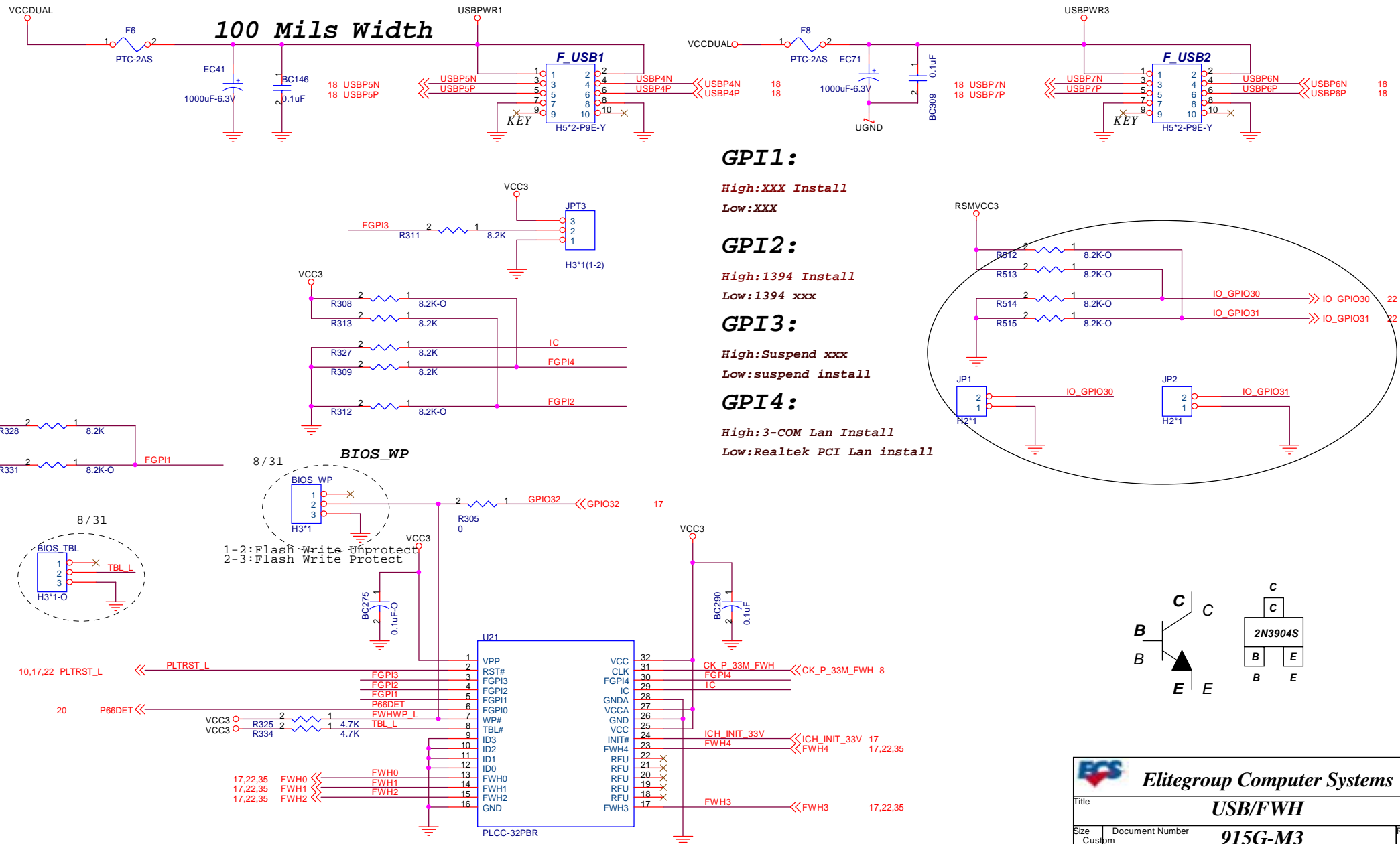




# MAX TRACE LENGTH IS 8"

DATA LINES SHOULD BE MATCHED TO STROBES ( XDIOR\_L , XIORDY\_L ) WITHIN +/- 250 MIL,  
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.

# USB PORT INTERFACE



## GPI1:

High:XXX Install

Low:XXX

## GPI2:

High:1394 Install

Low:1394 xxx

## GPI3:

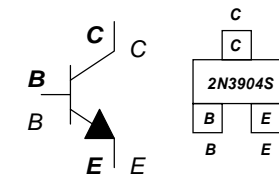
High:Suspend xxx

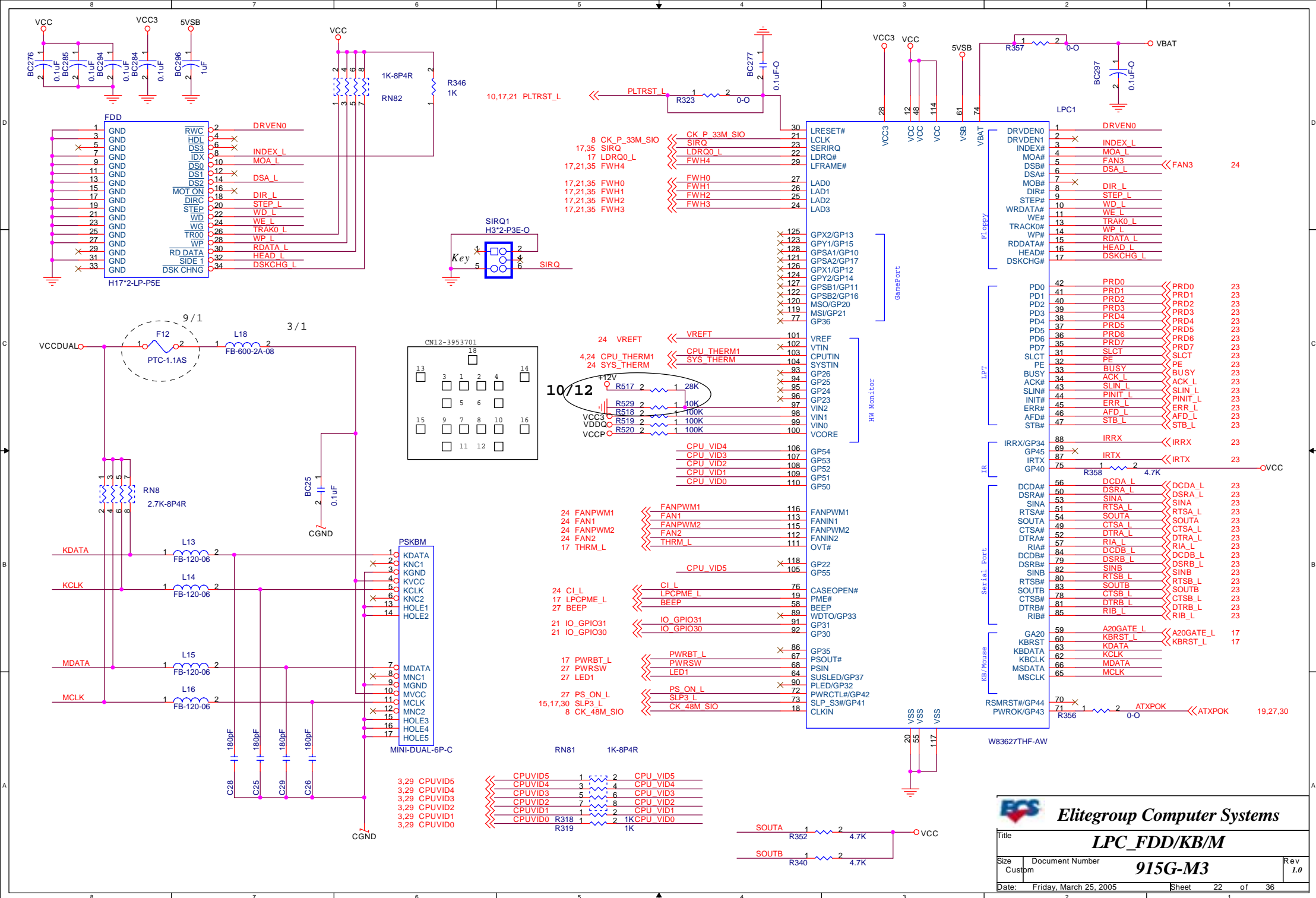
Low:suspend install

## GPI4:

High:3-COM Lan Install

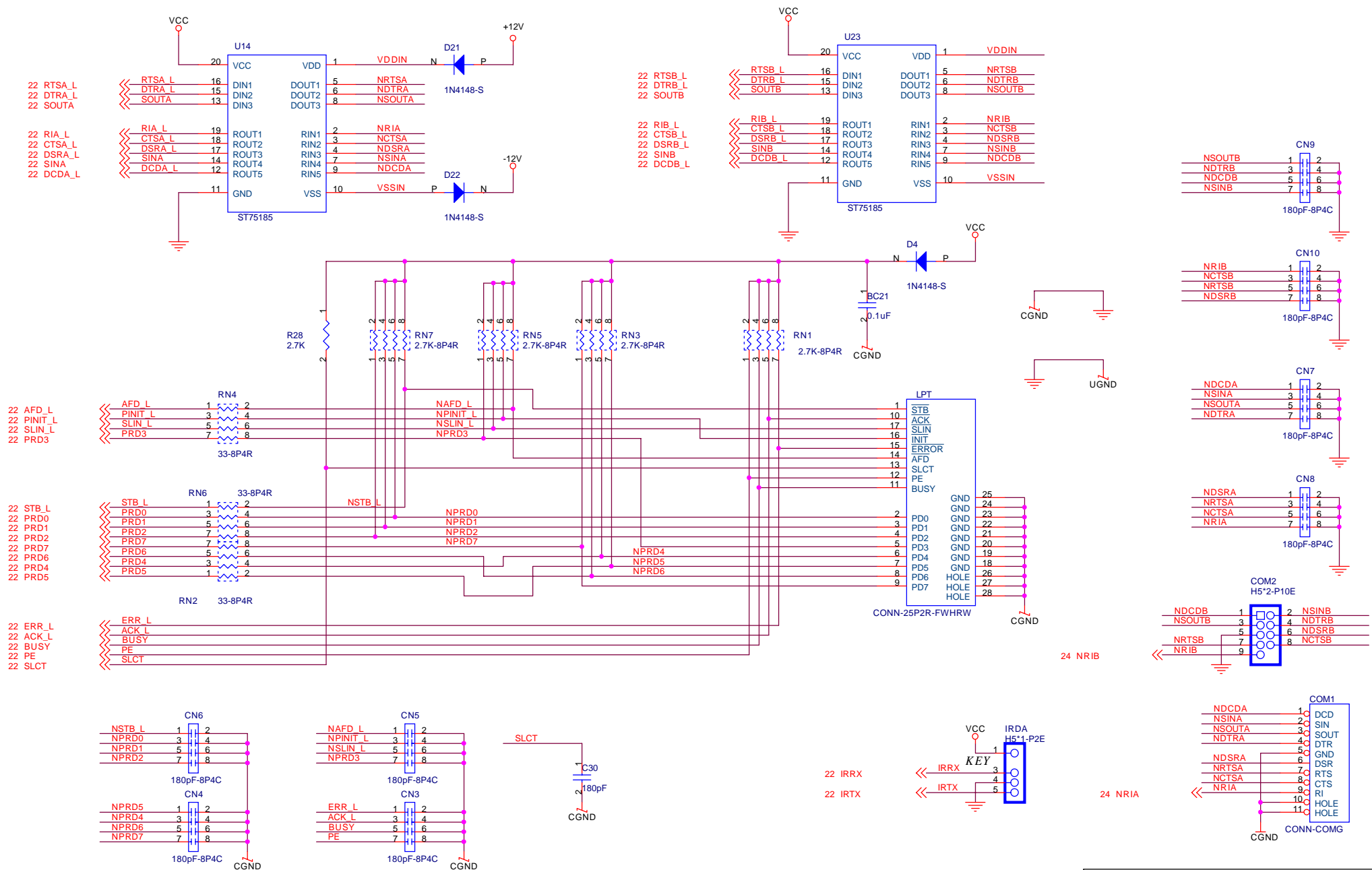
Low:Realtek PCI Lan install

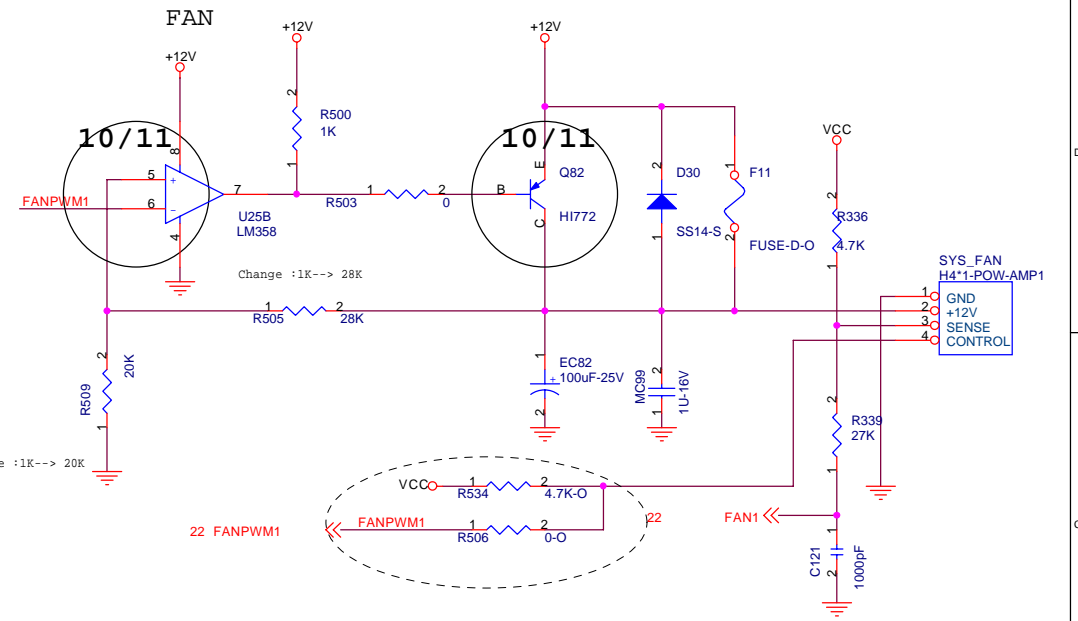
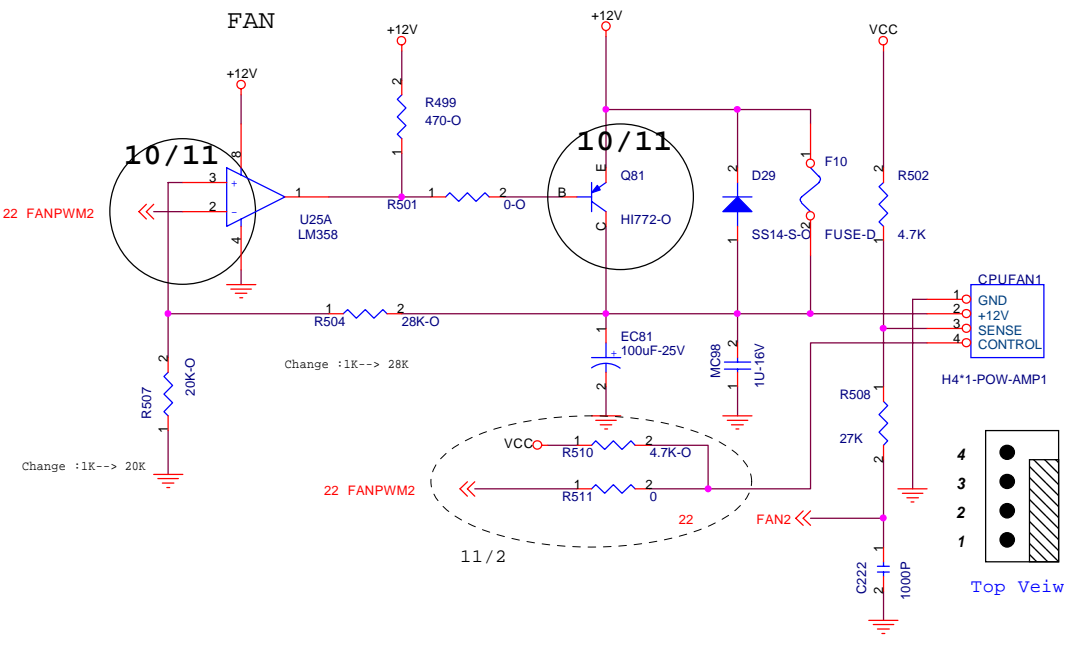




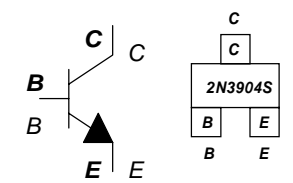
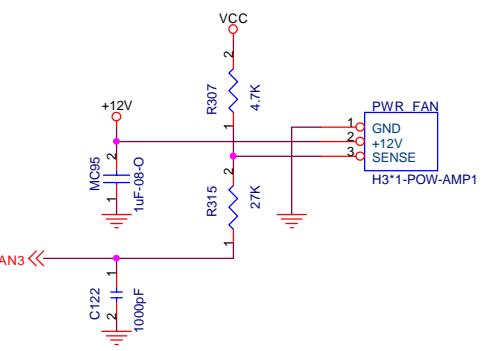
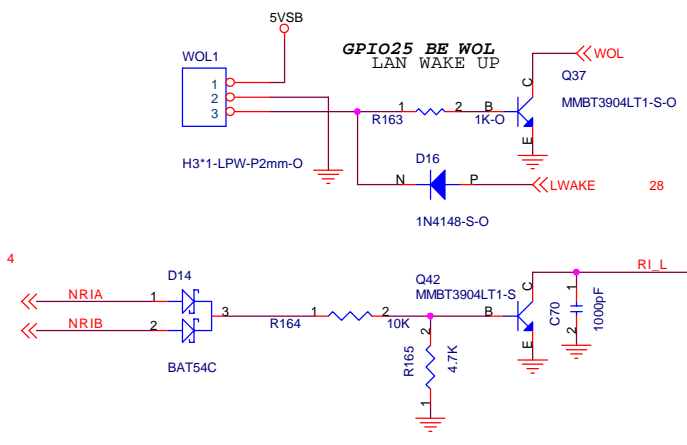
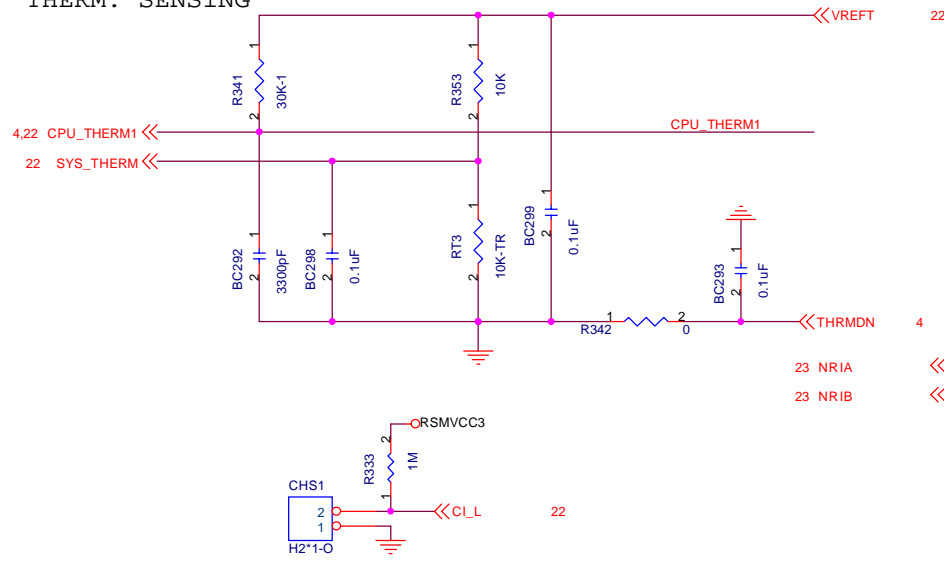
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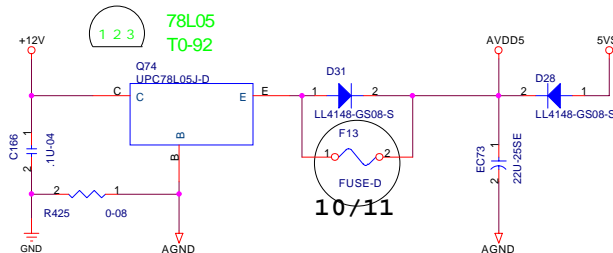
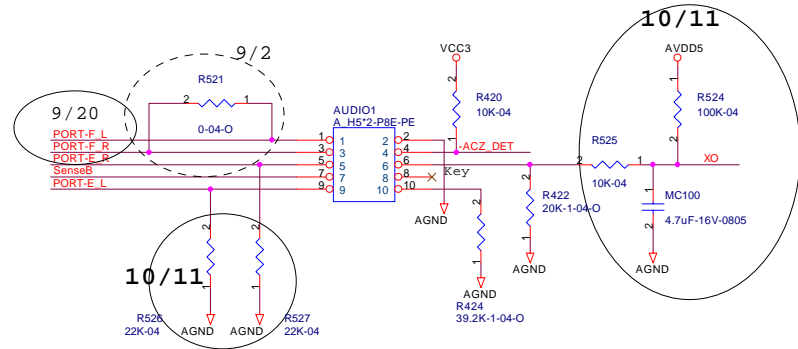
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Size	Document Number			<b><i>915G-M3</i></b>	Rev	<b><i>1.0</i></b>	
	Custom						
Date:	Friday, March 25, 2005			Sheet	22	of	36





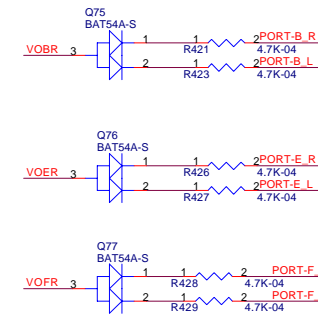
# THERM. SENSING



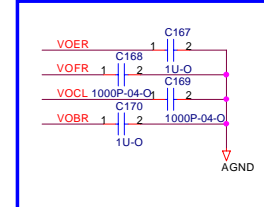


# Verfourt bias for stereo microphone.

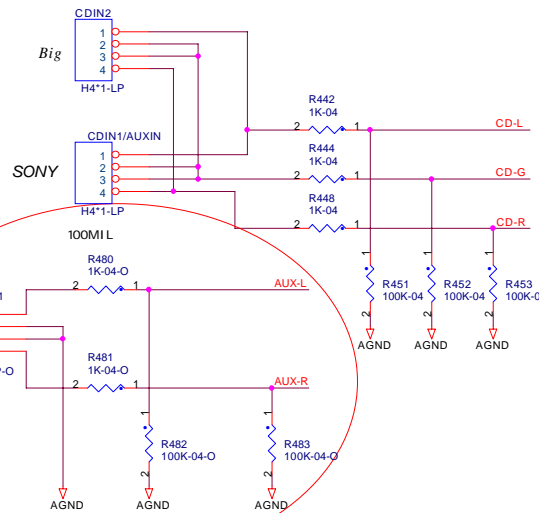
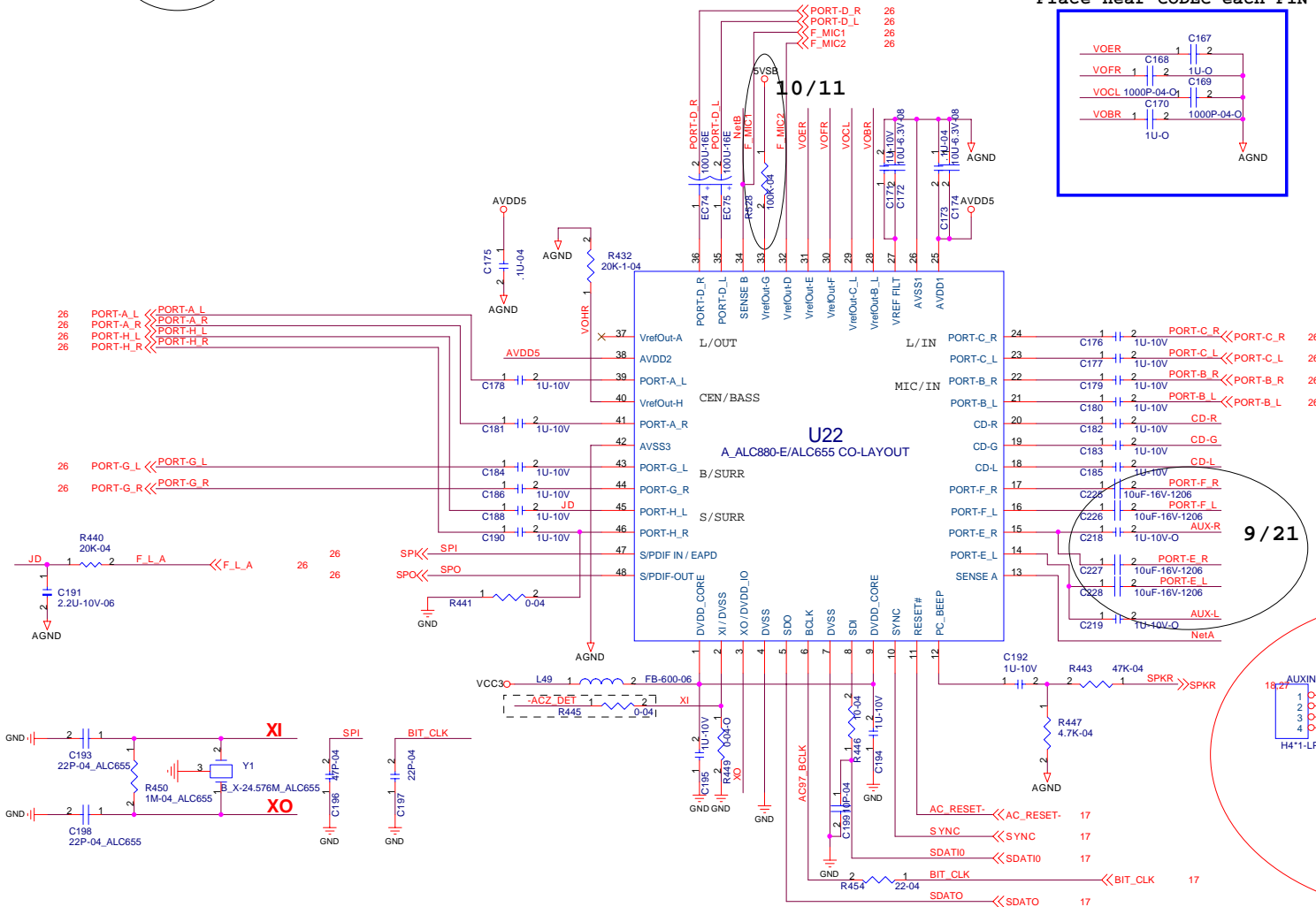
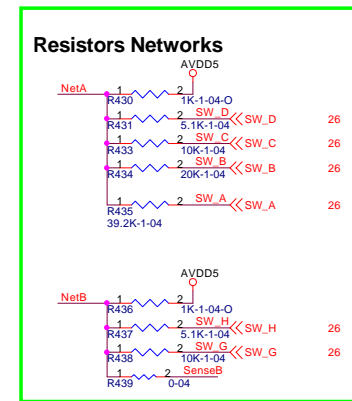
For CMI9880



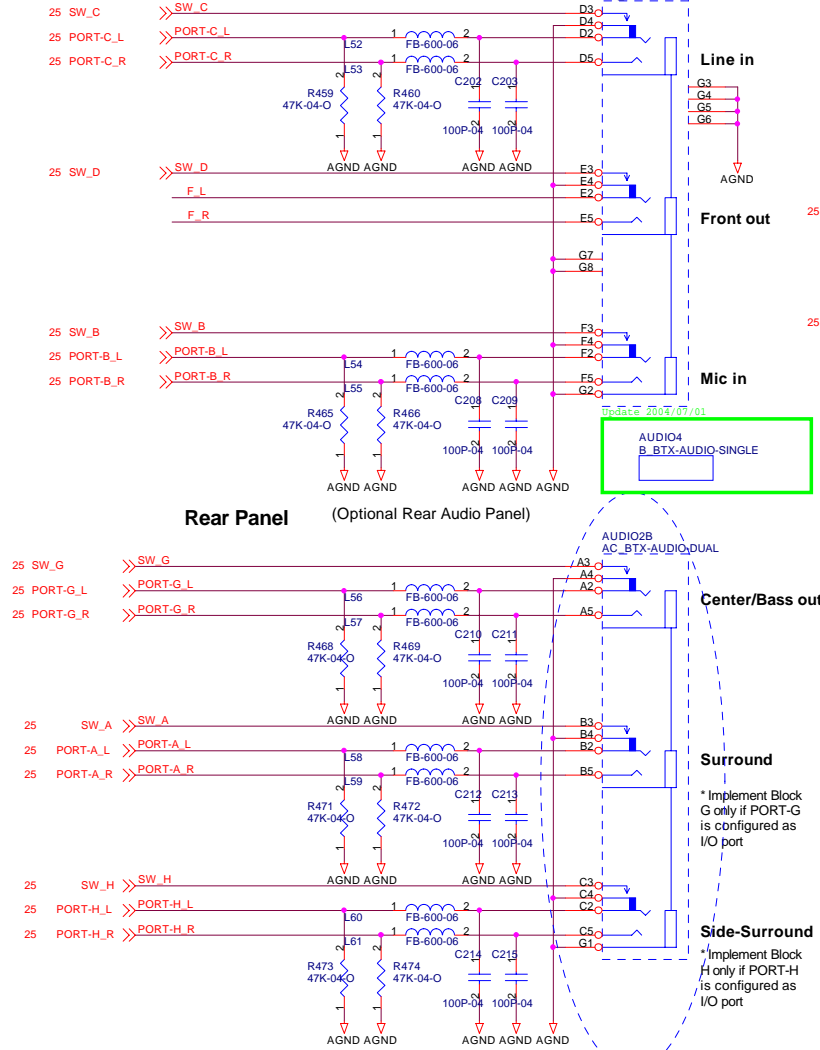
Place near CODEC each PIN



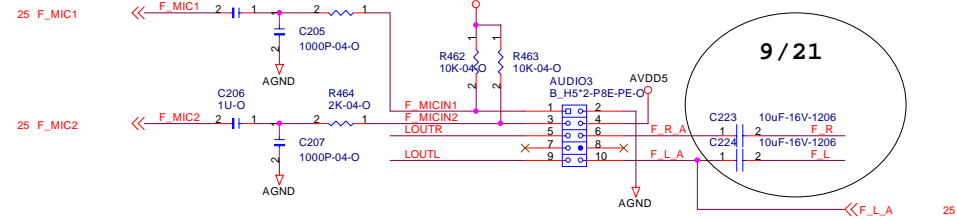
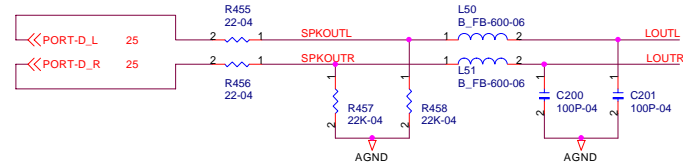
Place near Chip ( U23 )



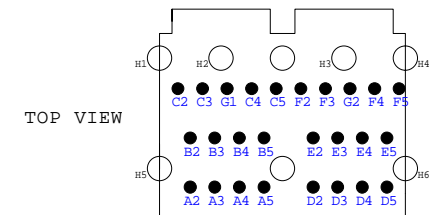
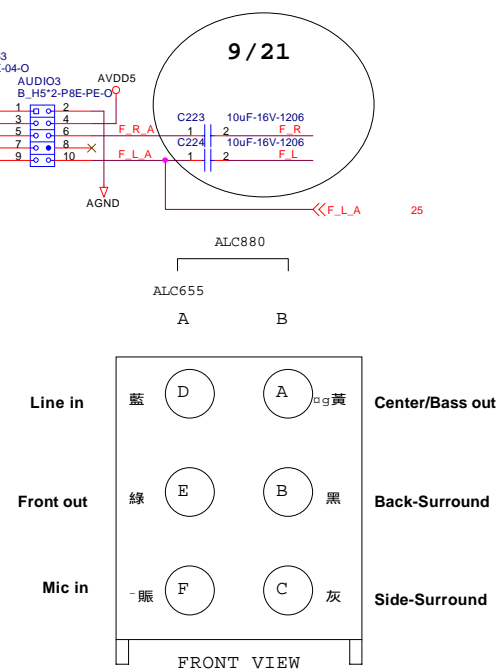
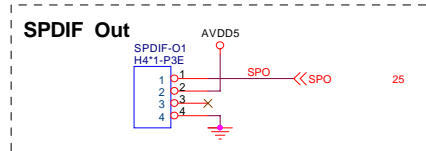
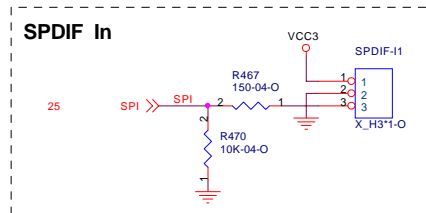
# Rear Panel Onboard Analog I/O

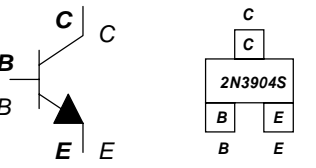
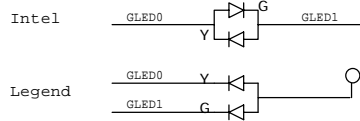
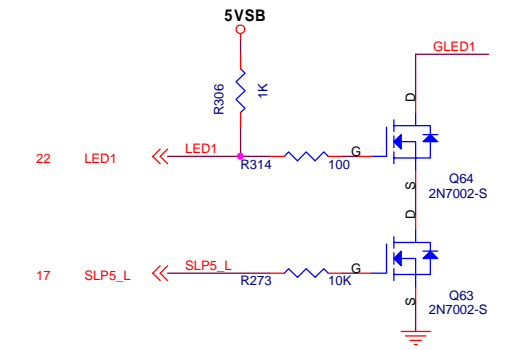
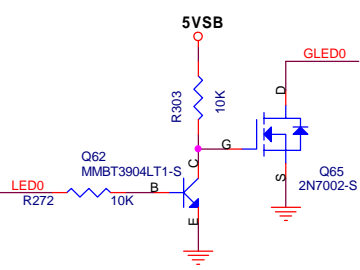
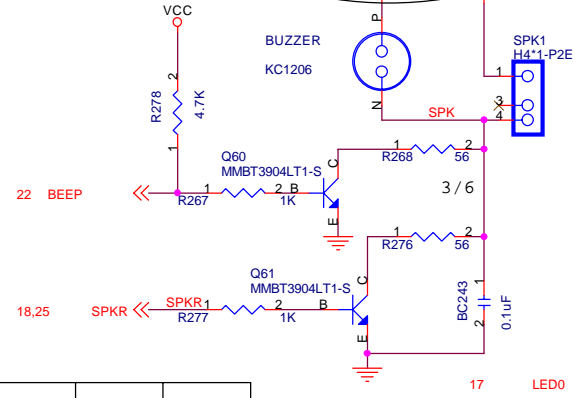
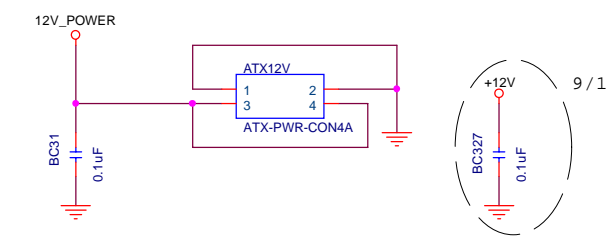
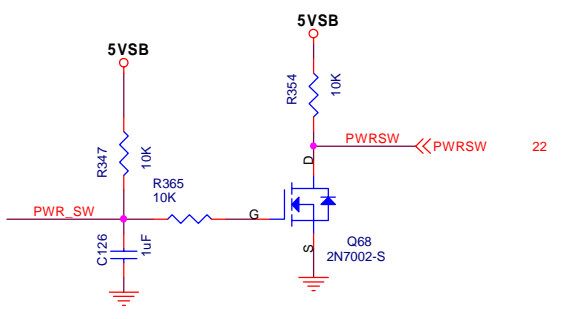
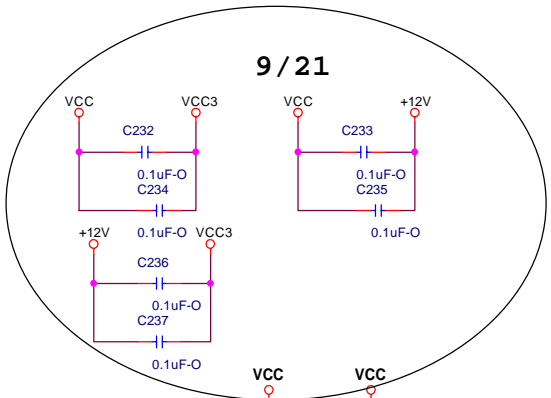
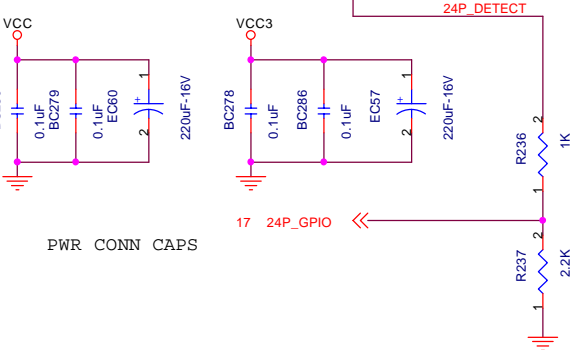
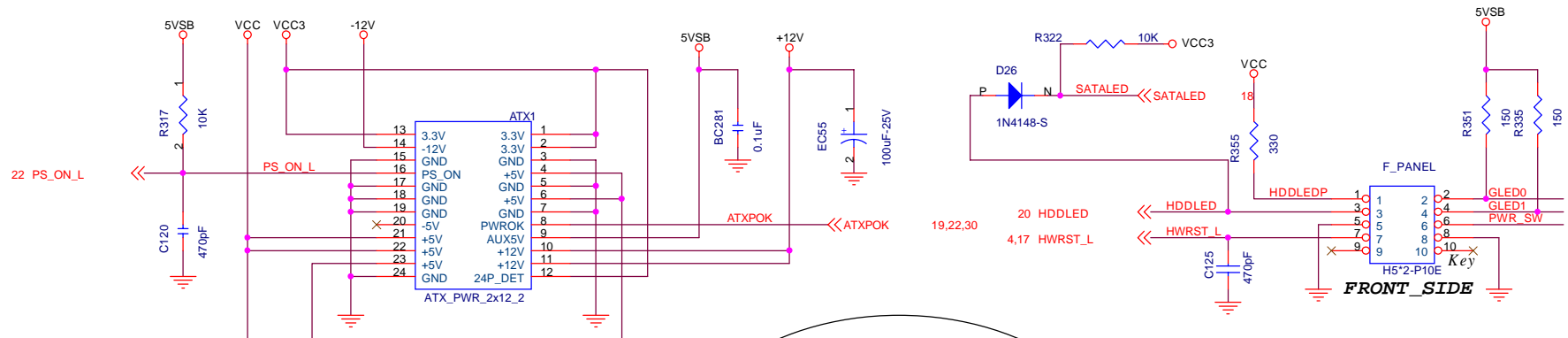


The schematic should consist with PINs define of I/O connector.

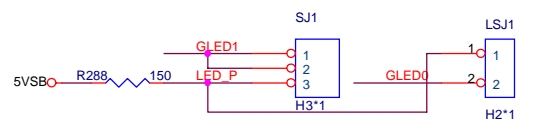


## SPDIF I/O





	S0	S1	S3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,S,7)	Green	G-blinking	G-blinking	Dark
LSJ1(1,2)	Dark	Dark	Light	Dark
SJ1(1,3)(2,3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH



**Elitegroup Computer Systems**

**ATX Power & Front Panel**

Size B

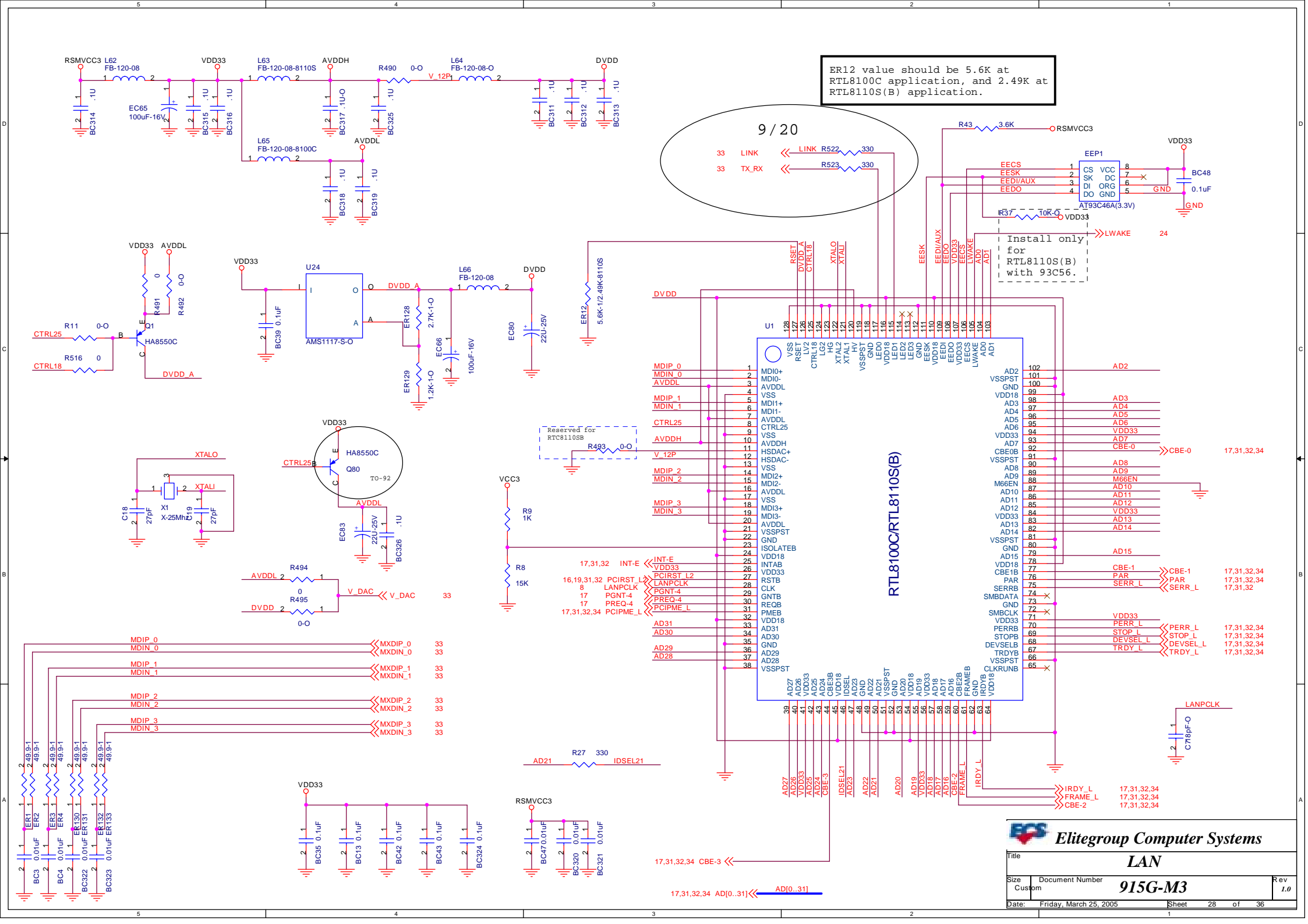
Document Number

915G-M3

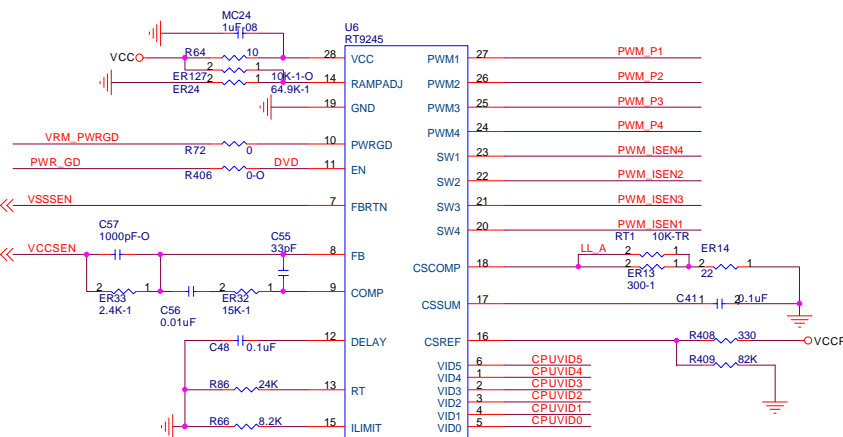
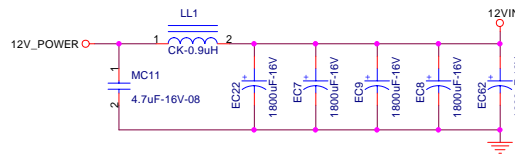
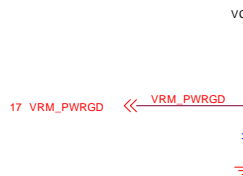
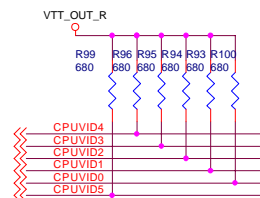
Rev 1.0

Date: Friday, March 25, 2005

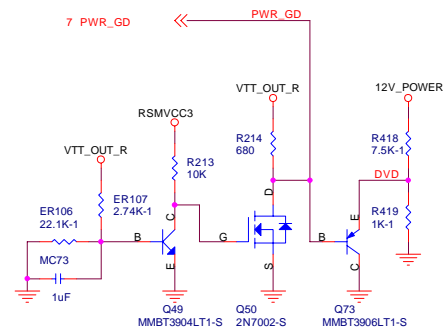
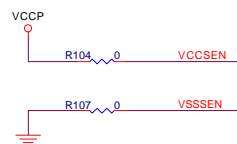
Sheet 27 of 36



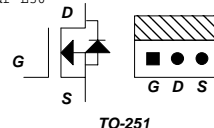
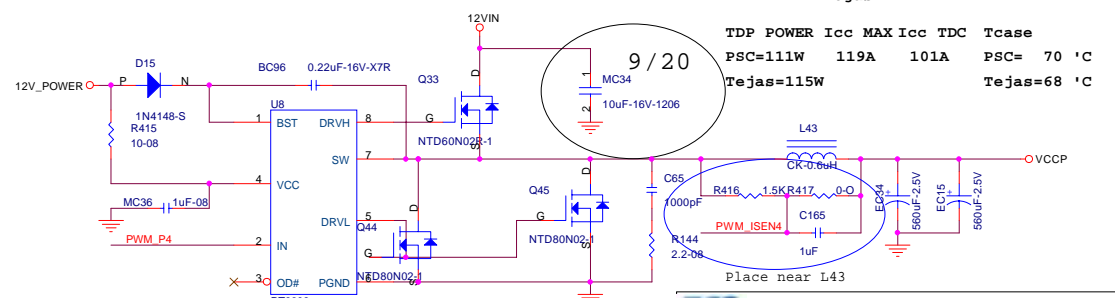
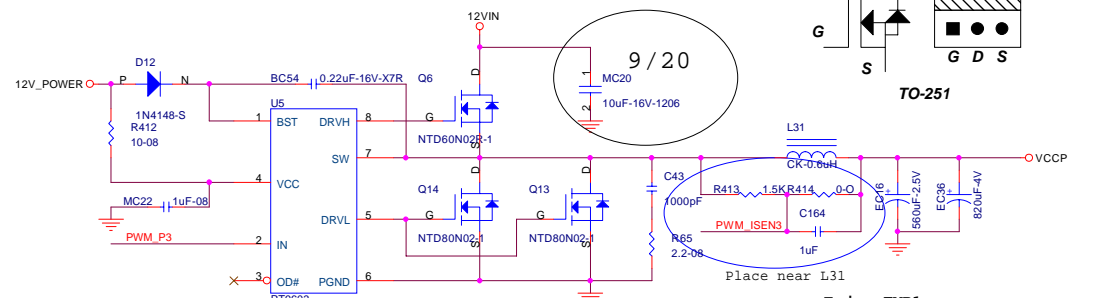
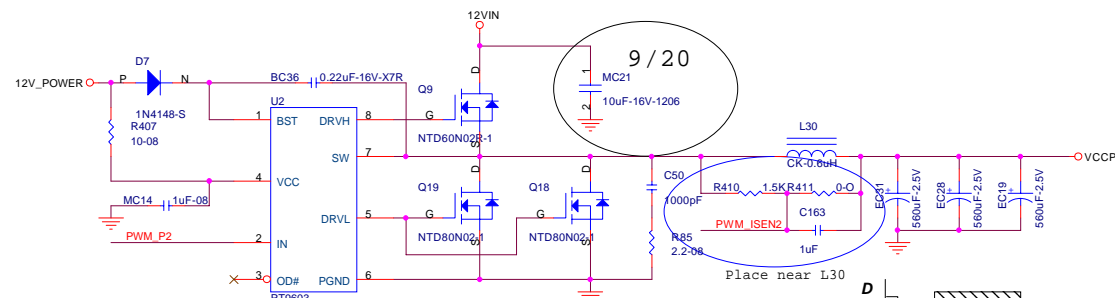
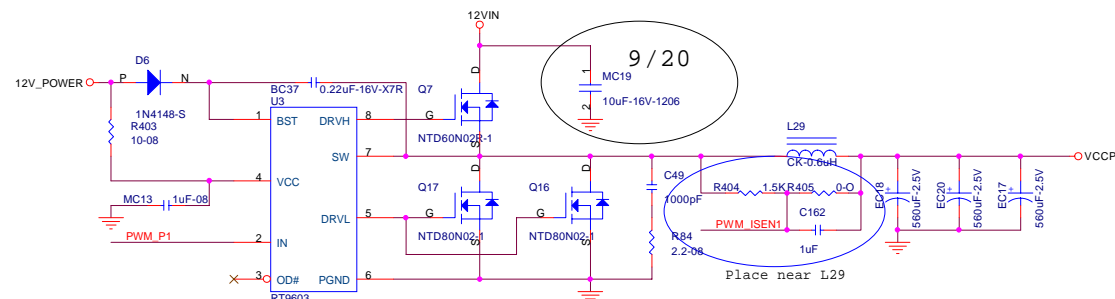
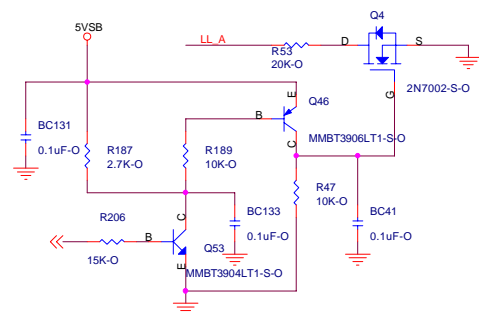
3.22 CPUVID4  
3.22 CPUVID3  
3.22 CPUVID2  
3.22 CPUVID1  
3.22 CPUVID0  
3.22 CPUVID5



3 VSSSEN  
3 VCCSEN

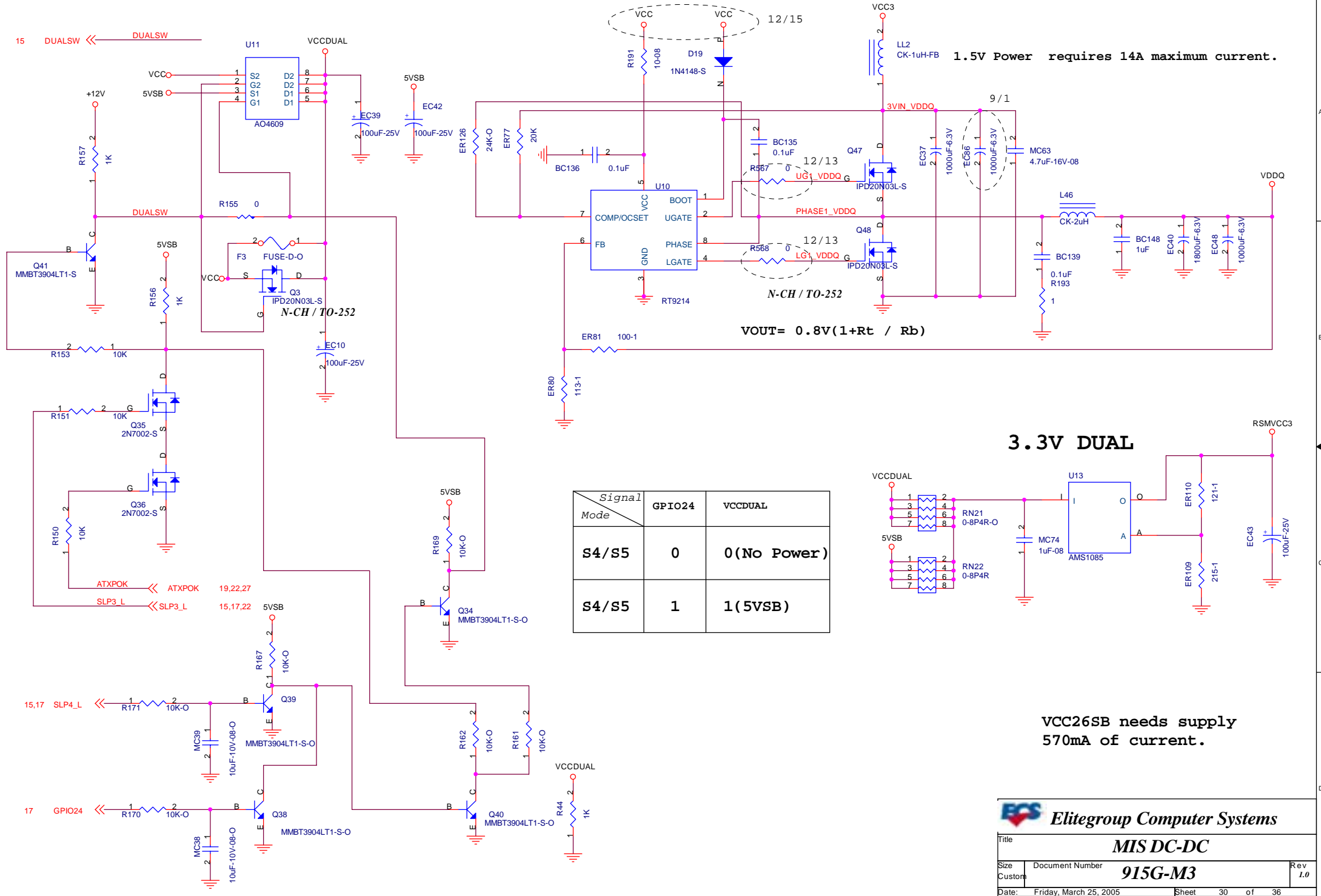


4 LL\_ID0



Tejas FMB1

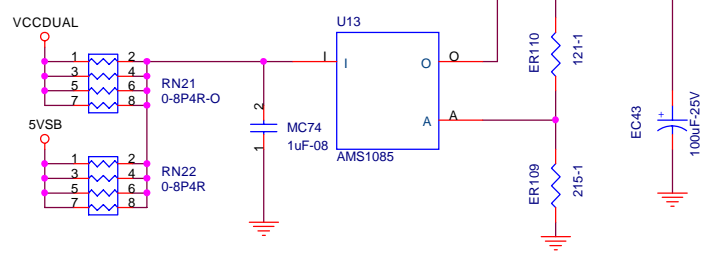
TDP POWER Icc MAX Icc TDC Tcase  
PSC=111W 119A 101A PSC= 70 °C  
Tejas=115W Tejas=68 °C



1.5V Power requires 14A maximum current.

$VOUT = 0.8V(1 + R_t / R_b)$

3.3V DUAL

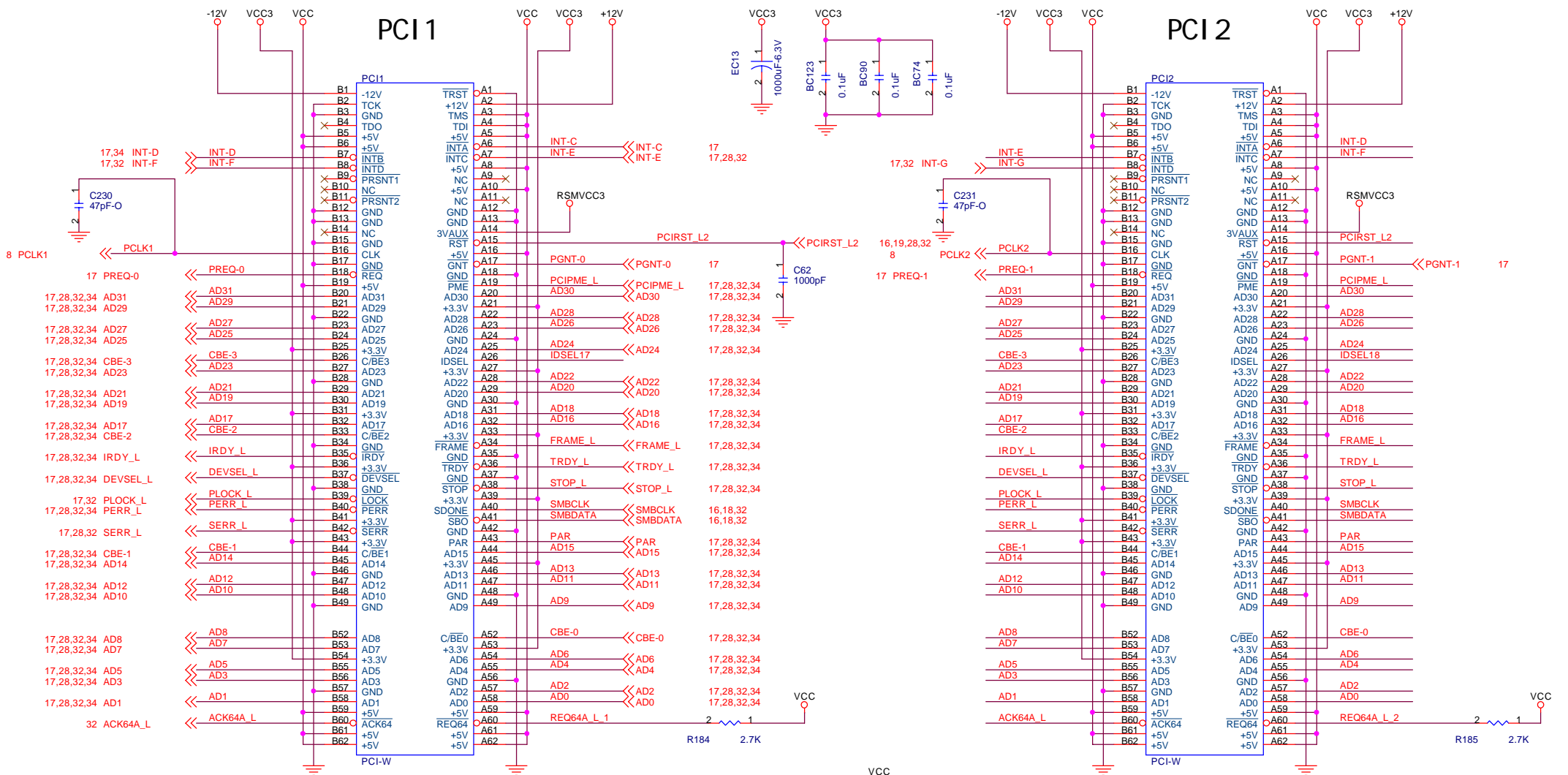


VCC26SB needs supply 570mA of current.

Signal Mode	GPIO24	VCCDUAL
S4/S5	0	0(No Power)
S4/S5	1	1(5VSB)

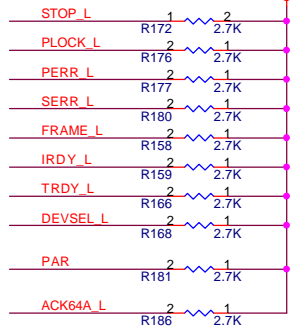
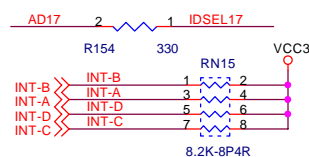
# PCI 1

# PCI 2



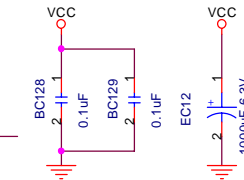
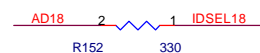
PCI1-INT:  
INTA:INTC  
INTB:INTD  
INTC:INTE  
INTD:INTF

IDSEL=AD17  
REQ=PREQ0#  
GNT=PGNT0#



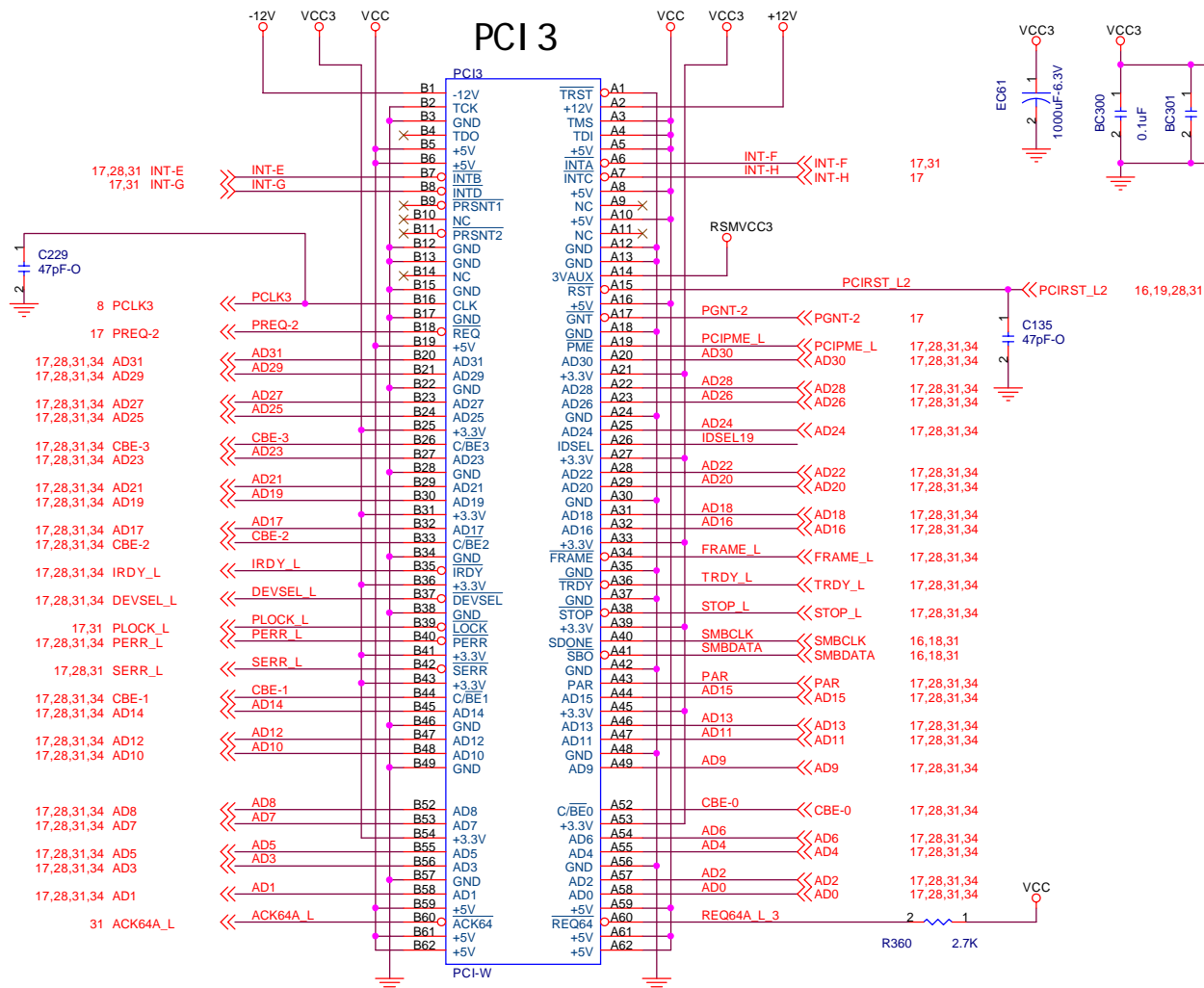
PCI2-INT:  
INTA:INTD  
INTB:INTE  
INTC:INTF  
INTD:INTG

IDSEL=AD18  
REQ=PREQ1#  
GNT=PGNT1#

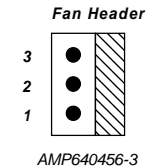
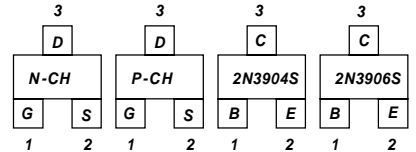
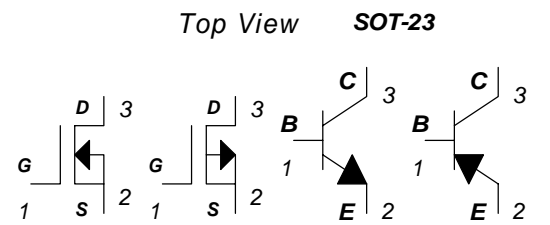
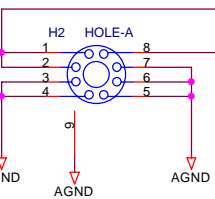
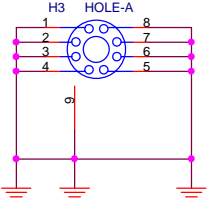
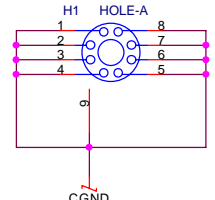
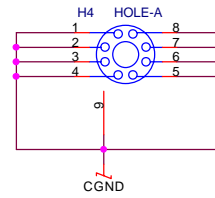
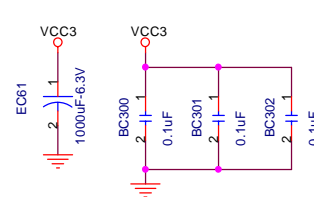
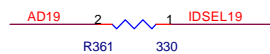


Elitegroup Computer Systems

Title			PCI Slot 1&2		
Size	Document Number	915G-M3			Rev
Custom					L.0
Date:	Friday, March 25, 2005	Sheet	31	of	36

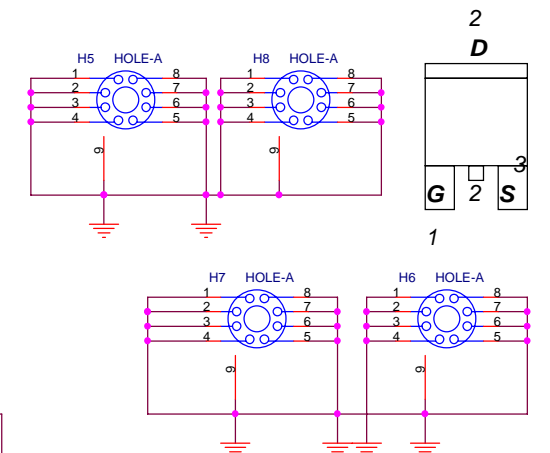
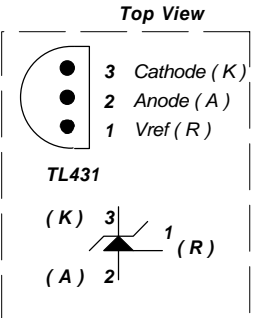
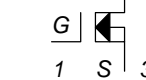


PCI 3 - INT: IDSEL=AD19  
 INTA: INTF REQ=PREQ2#  
 INTB: INTF GNT=PGNT2#  
 INTC: INTG  
 INTD: INTF



AMP640456-3

TO-263 / TO-252

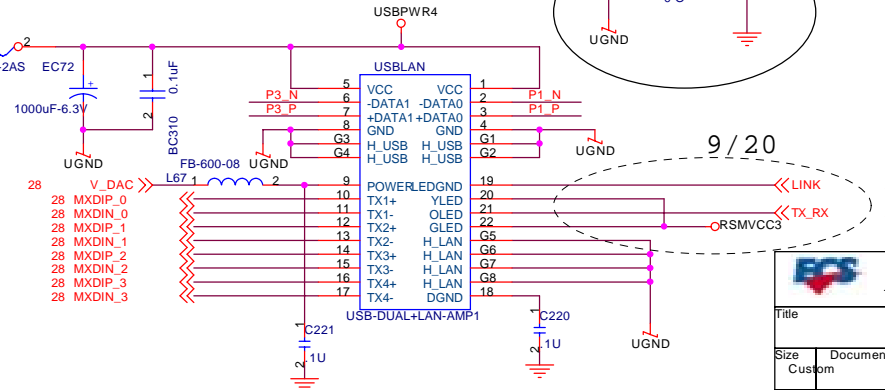
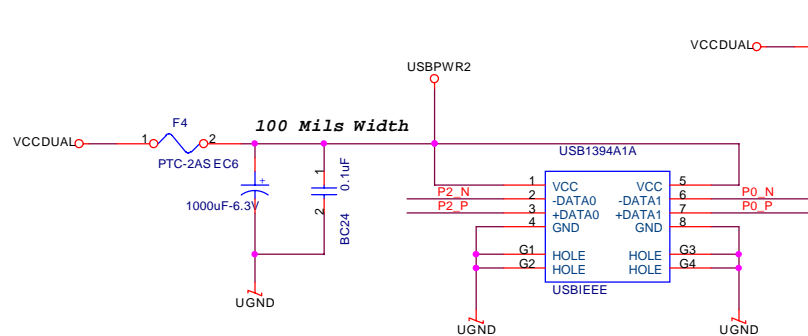
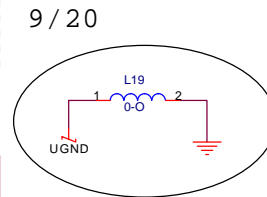
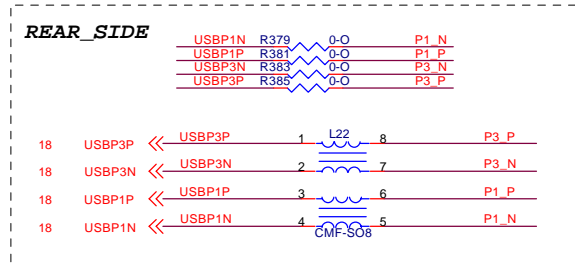
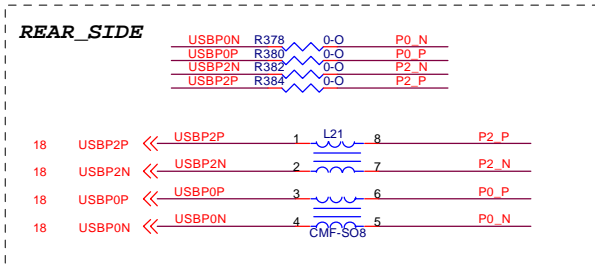
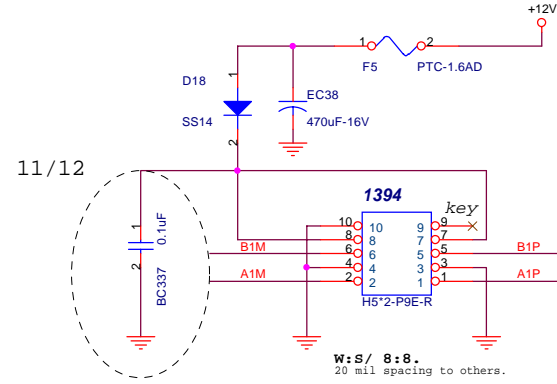
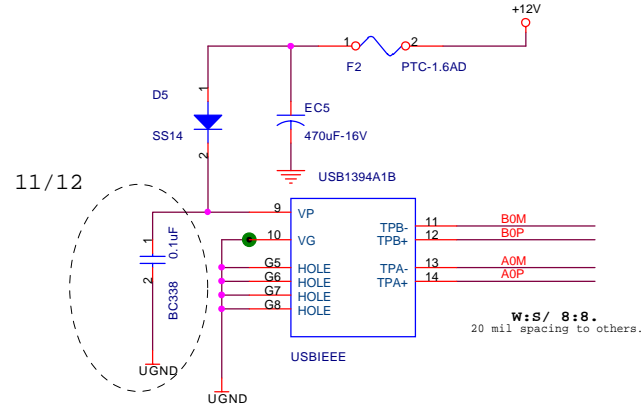
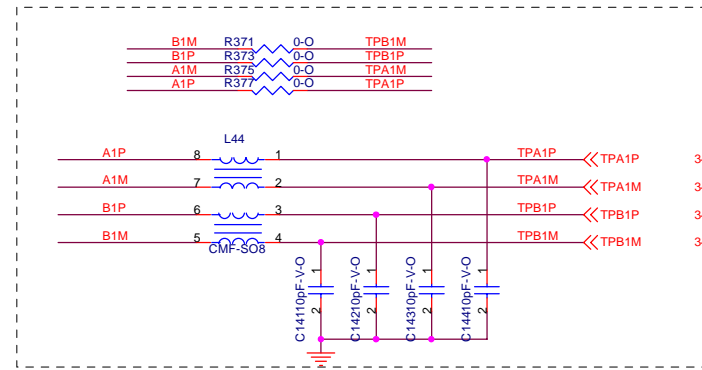
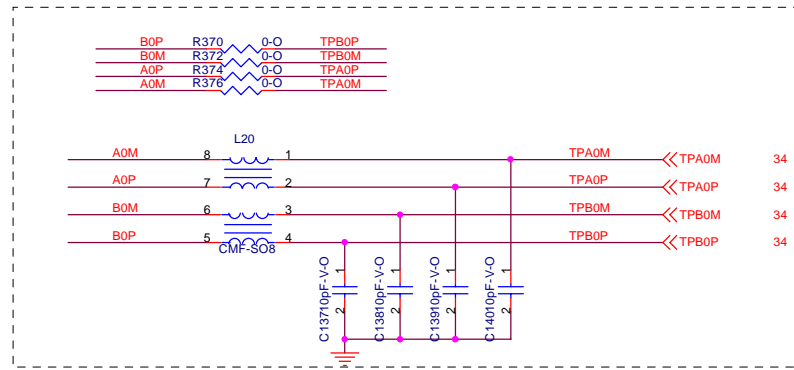


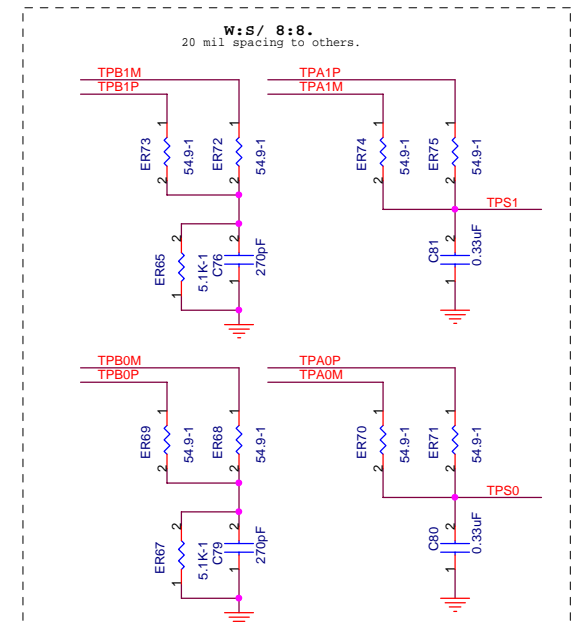
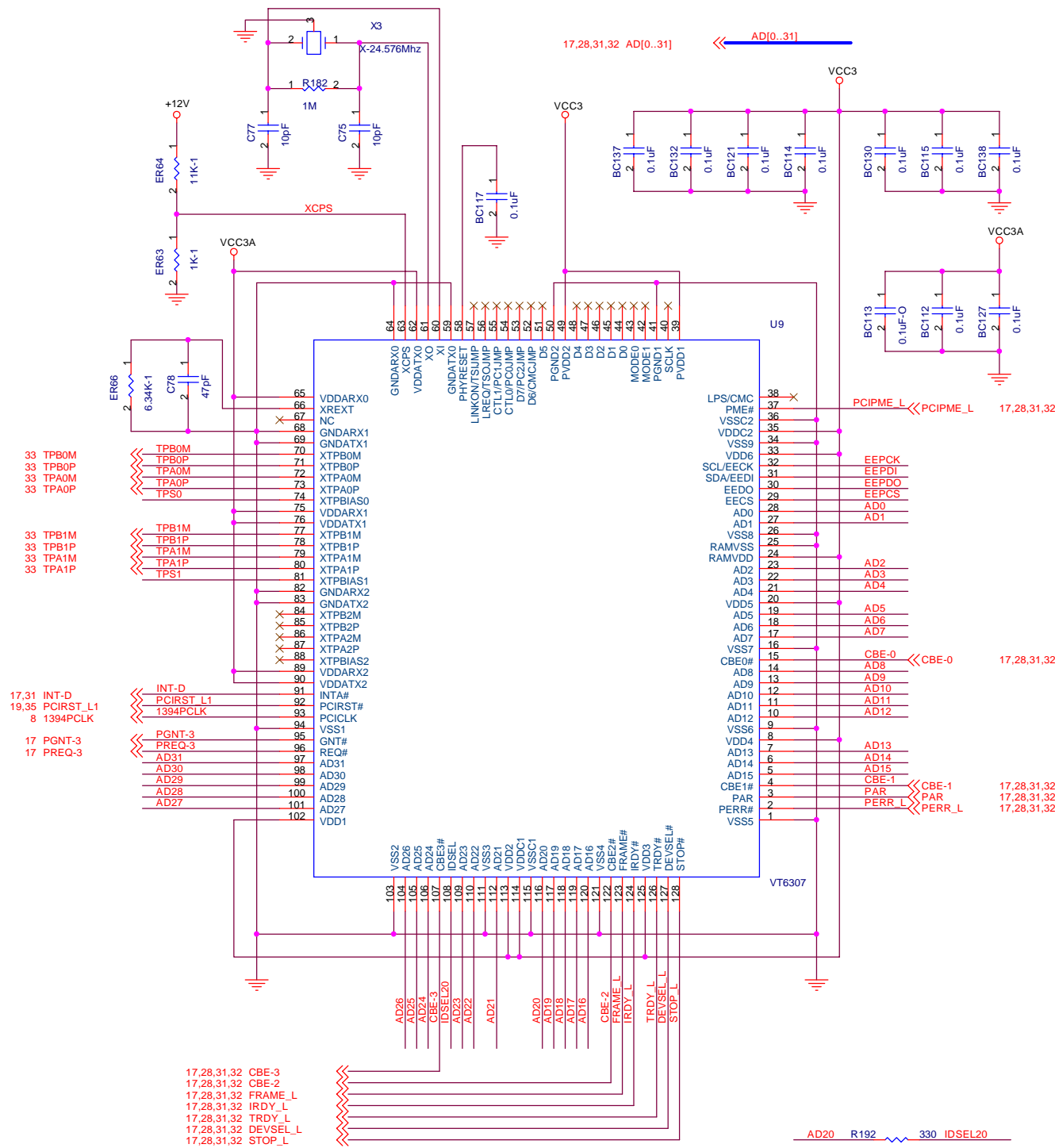
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Title: **PCI Slot 3**

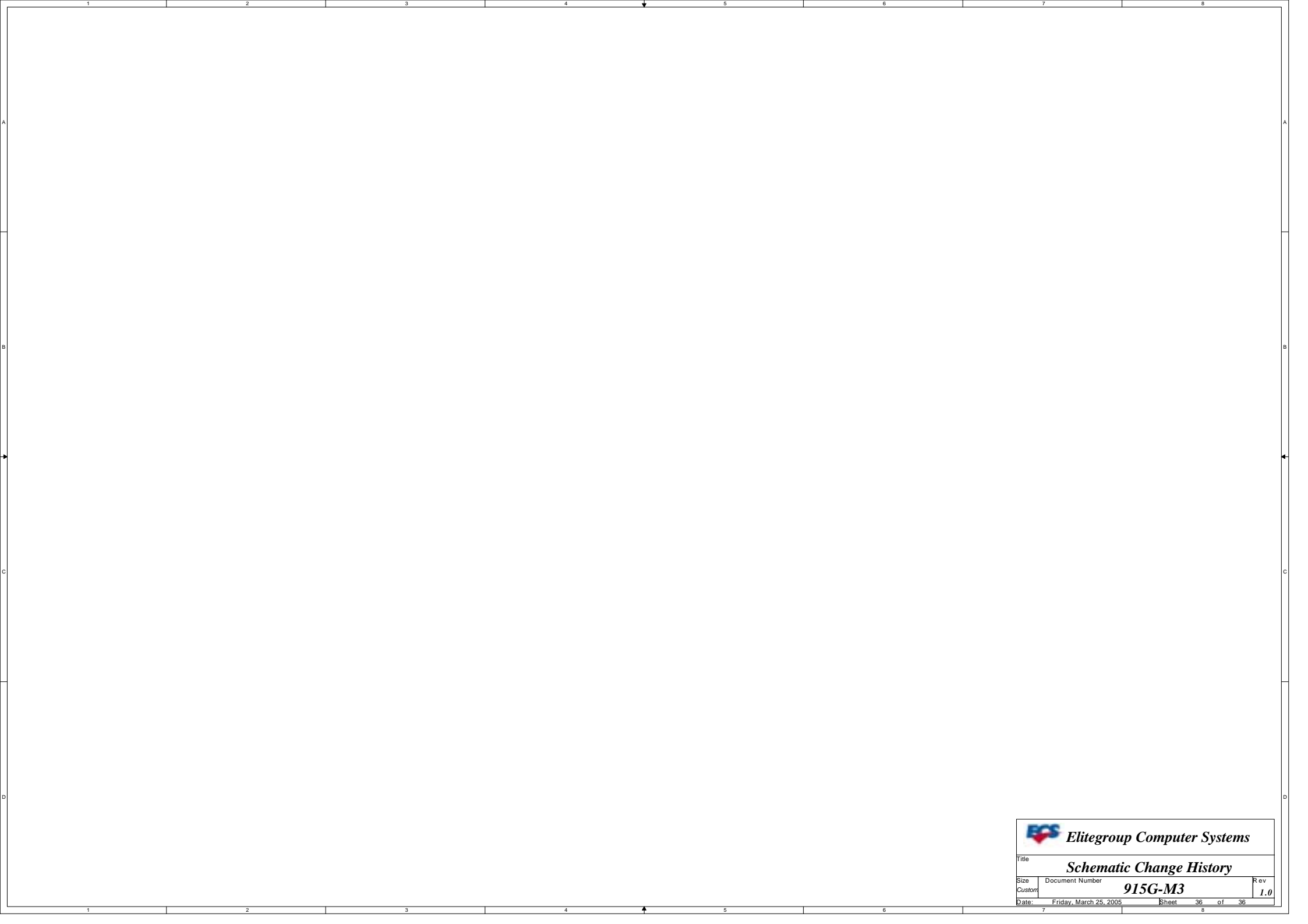
Size B Document Number: **915G-M3** Rev 1.0


Date: Friday, March 25, 2005 Sheet 32 of 36









 <b>Elitegroup Computer Systems</b>		
Title <b>Schematic Change History</b>		
Size Custom	Document Number <b>915G-M3</b>	Rev <b>1.0</b>
Date: Friday, March 25, 2005	Sheet 36 of 36	